

# MEMORY Mobile FCRAM™

CMOS

## 128 M Bit (8 M word×16 bit) Mobile Phone Application Specific Memory

### MB82DBS08164D-70L

#### ■ DESCRIPTION

The FUJITSU MICROELECTRONICS MB82DBS08164D is a CMOS Fast Cycle Random Access Memory (FCRAM\*) with asynchronous Static Random Access Memory (SRAM) interface containing 134,217,728 storages accessible in a 16-bit format.

The MB82DBS08164D adopts asynchronous mode and synchronous burst mode for fast memory access as user configurable options.

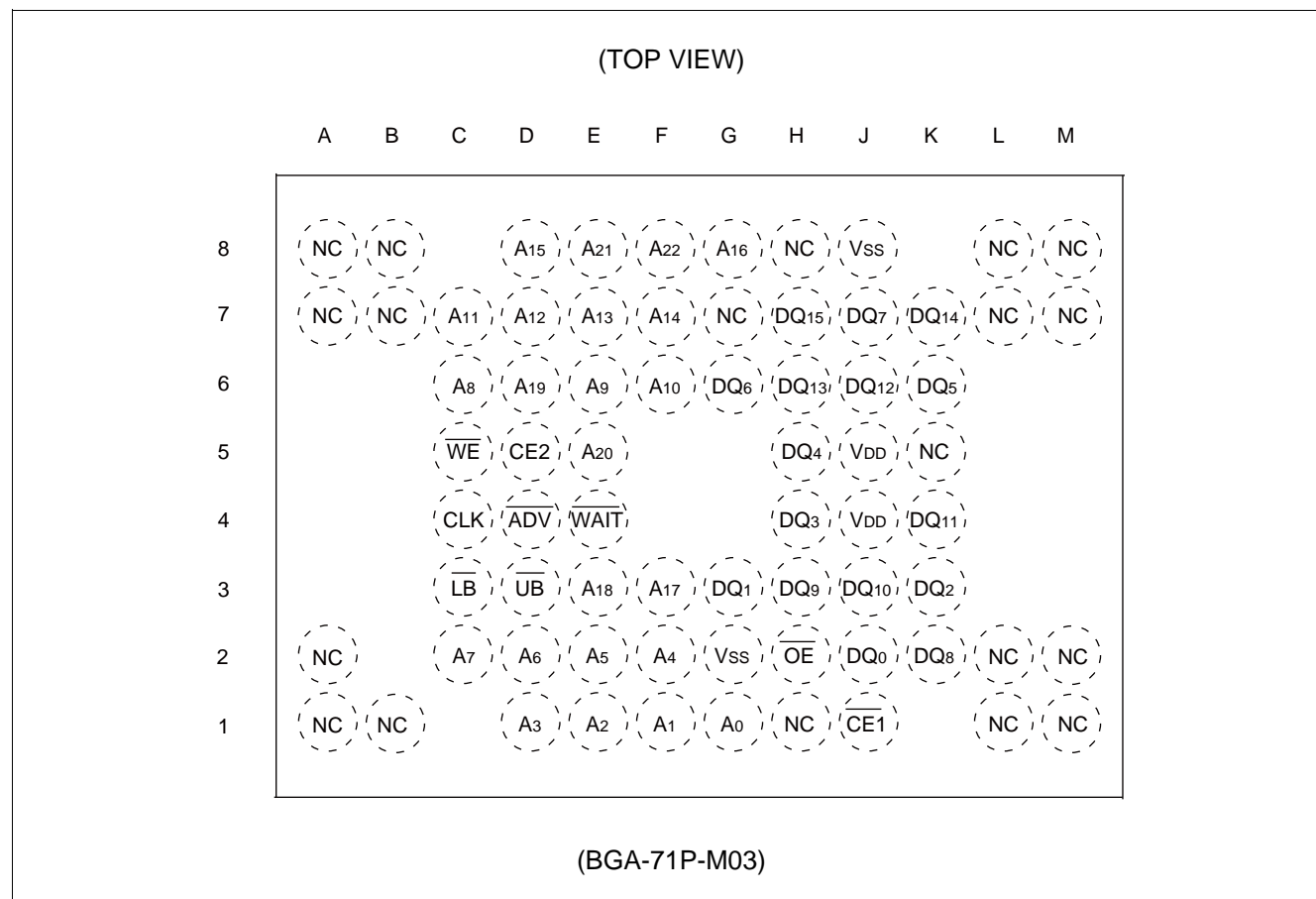
The MB82DBS08164D is suited for mobile applications such as Cellular Handset and PDA.

\* : FCRAM is a trademark of Fujitsu Microelectronics Limited, Japan

#### ■ FEATURES

- Asynchronous SRAM Interface
- COSMORAM Revision 3 Compliance  
(COSMORAM : Common Specifications of Mobile RAM)
- Fast Access Time :  $t_{CE} = 70$  ns Max
- Burst Read/Write Access Capability :  
 $t_{CK} = 13$  ns Min / 77 MHz Max  
 $t_{AC} = 6$  ns Max
- Low Voltage Operating Condition :  $V_{DD} = 1.7$  V to 1.95 V
- Wide Operating Temperature :  $T_A = 0$  °C to + 70 °C
- Byte Control by  $\overline{LB}$  and  $\overline{UB}$
- Low-Power Consumption :  $I_{DDA1} = 35$  mA Max  
 $I_{DDs1} = 200$   $\mu$ A Max ( $T_A \leq + 40$  °C)
- Various Power Down mode : Sleep
  - 16 M-bit Partial
  - 32 M-bit Partial
  - 64 M-bit Partial

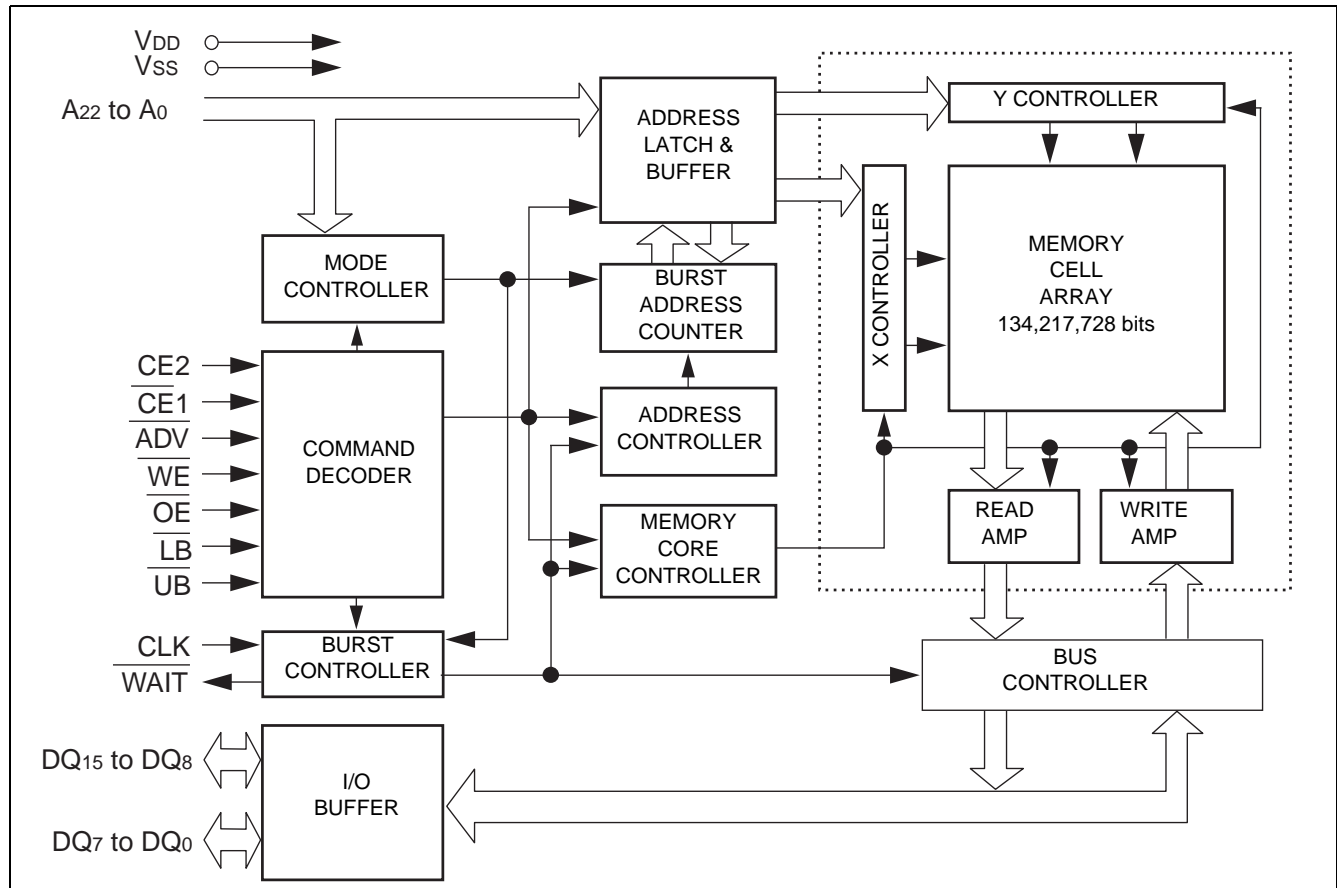
## PIN ASSIGNMENT



## PIN DESCRIPTION

Pin Name	Description
A <sub>22</sub> to A <sub>0</sub>	Address Input
$\overline{\text{CE}}1$	Chip Enable 1 (Low Active)
CE2	Chip Enable 2(High Active)
$\overline{\text{WE}}$	Write Enable (Low Active)
$\overline{\text{OE}}$	Output Enable (Low Active)
$\overline{\text{LB}}$	Lower Byte Control (Low Active)
$\overline{\text{UB}}$	Upper Byte Control (Low Active)
CLK	Clock Input
$\overline{\text{ADV}}$	Address Valid Input (Low Active)
$\overline{\text{WAIT}}$	Wait Output
DQ <sub>7</sub> to DQ <sub>0</sub>	Lower Byte Data Input/Output
DQ <sub>15</sub> to DQ <sub>8</sub>	Upper Byte Data Input/Output
V <sub>DD</sub>	Power Supply Voltage
V <sub>SS</sub>	Ground
NC	No Connection

## ■ BLOCK DIAGRAM



## ■ FUNCTION TRUTH TABLE

### 1. Asynchronous Operation

Mode	CE2	$\overline{CE1}$	CLK	$\overline{ADV}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	A <sub>22</sub> to A <sub>0</sub>	DQ <sub>7</sub> to DQ <sub>0</sub>	DQ <sub>15</sub> to DQ <sub>8</sub>	$\overline{WAIT}$
Standby (Deselect)	H	H	X	X	X	X	X	X	X	High-Z	High-Z	High-Z
Output Disable*1	H	L	X	*3	H	H	X	X	*5	High-Z	High-Z	High-Z
Output Disable (No Read)			X	*3	H	L	H	H	Valid	High-Z	High-Z	High-Z
Read (Upper Byte)			X	*3			H	L	Valid	High-Z	Output Valid	High-Z
Read (Lower Byte)			X	*3			L	H	Valid	Output Valid	High-Z	High-Z
Read (Word)			X	*3			L	L	Valid	Output Valid	Output Valid	High-Z
No Write			X	*3	L	H*4	H	H	Valid	Invalid	Invalid	High-Z
Write (Upper Byte)			X	*3			H	L	Valid	Invalid	Input Valid	High-Z
Write (Lower Byte)			X	*3			L	H	Valid	Input Valid	Invalid	High-Z
Write (Word)			X	*3			L	L	Valid	Input Valid	Input Valid	High-Z
Power Down*2	L	X	X	X	X	X	X	X	X	High-Z	High-Z	High-Z

Note : L = V<sub>IL</sub>, H = V<sub>IH</sub>, X can be either V<sub>IL</sub> or V<sub>IH</sub>, High-Z = High Impedance

\*1 : Should not be kept this logic condition longer than 1  $\mu$ s.

\*2 : Power Down mode can be entered from Standby state and all output are in High-Z state.  
Data retention depends on the selection of Partial Size for Power Down Program. Refer to "Power Down" in "■FUNCTIONAL DESCRIPTION" for the details.

\*3 : "L" for address pass through and "H" for address latch on the rising edge of  $\overline{ADV}$ .

\*4 :  $\overline{OE}$  can be V<sub>IL</sub> during write operation if the following conditions are satisfied;

- (1) Write pulse is initiated by  $\overline{CE1}$ . Refer to "(12) Asynchronous Read/Write Timing 1-1 ( $\overline{CE1}$  Control)" in "■TIMING DIAGRAMS".
- (2)  $\overline{OE}$  stays V<sub>IL</sub> during Write cycle.

\*5 : Can be either V<sub>IL</sub> or V<sub>IH</sub> but must be valid before Read or Write.

## 2. Synchronous Operation (Burst Mode)

Mode	CE2	CE1	CLK	ADV	WE	OE	LB	UB	A <sub>22</sub> to A <sub>0</sub>	DQ <sub>15</sub> to DQ <sub>0</sub>	WAIT
Standby(Deselect)	H	H	X	X	X	X	X	X	X	High-Z	High-Z
Start Address Latch*1		L	*3 $\uparrow$	L	X*4	X*6	X*7	X*7	Valid*8	High-Z*9	Output Invalid
Advance Burst Read to Next Address*1			*3 $\uparrow$	H	H	L			X	Output Valid*10	Output Valid
Burst Read Suspend*1			*3 $\uparrow$		H	H				High-Z	High*12
Advance Burst Write to Next Address*1			*3 $\uparrow$			H				Input Valid*11	High*13
Burst Write Suspend*1			*3 $\uparrow$		H*5	H				Input Invalid	High*12
Terminate Burst Read		$\uparrow$	X		H	X				High-Z	High-Z
Terminate Burst Write		$\uparrow$	X		X	H				High-Z	High-Z
Power Down*2	L	X	X	X	X	X	X	X	X	High-Z	High-Z

Note : L = V<sub>IL</sub>, H = V<sub>IH</sub>, X can be either V<sub>IL</sub> or V<sub>IH</sub>,  $\uparrow$  = valid edge, High-Z = High impedance

\*1 : Should not be kept this logic condition longer than 8  $\mu$ s.

\*2 : Power Down mode can be entered from Standby state and all output are in High-Z state.  
Data retention depends on the selection of Partial Size for Power Down Program.  
Refer to "Power Down" in "FUNCTIONAL DESCRIPTION" for the details.

\*3 : CLK must be started and stable prior to memory access.

\*4 : Can be V<sub>IH</sub> for the burst write operation in "WE Level Control" mode but must be V<sub>IL</sub> for the burst write operation in "WE Single Clock Pulse Control" mode. WE must be V<sub>IH</sub> for the burst read operation.

\*5 : When device is operating in "WE Single Clock Pulse Control" mode, WE is a "don't care" once write operation is determined by WE Low Pulse at the beginning of write access together with address latching. Burst write suspend feature is not supported in "WE Single Clock Pulse Control" mode.

\*6 : Can be V<sub>IL</sub> for the burst read operation but must be V<sub>IH</sub> for the burst write operation.

\*7 : Can be either V<sub>IL</sub> or V<sub>IH</sub>. During burst write operation, byte write control by LB and UB can be performed at each clock cycle. During read operation, LB and UB must be valid before read operation is initiated. And once LB and UB input levels are determined, they must not be changed until the end of burst read.

\*8 : Once a valid address is determined, the input address must not be changed during ADV = L.

\*9 : If OE = L, data output is either Invalid or High-Z depending on the level of LB and UB input. If WE = L, data input is Invalid. If OE = WE = H, data output is High-Z.

\*10 : Data output is either Valid or High-Z depending on the level of LB and UB input.

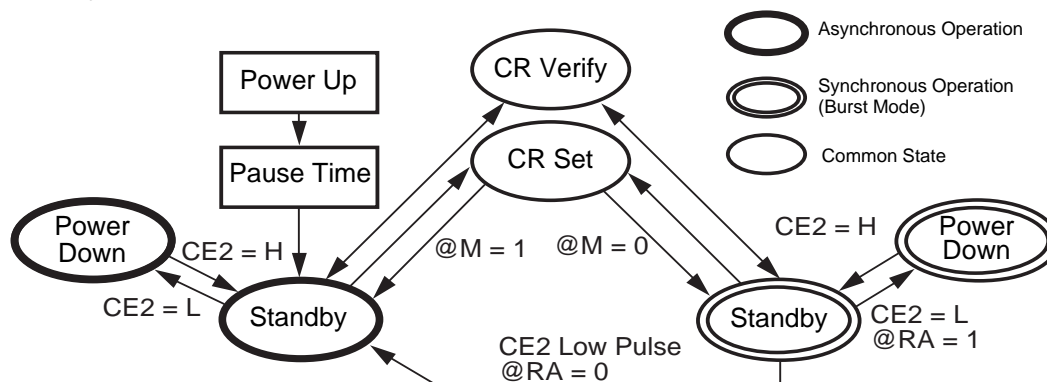
\*11 : Data input is either Valid or Invalid depending on the level of LB and UB input.

\*12 : Keep the level from previous cycle except for suspending on last data. Refer to "WAIT Output Function" in "FUNCTIONAL DESCRIPTION" for the details.

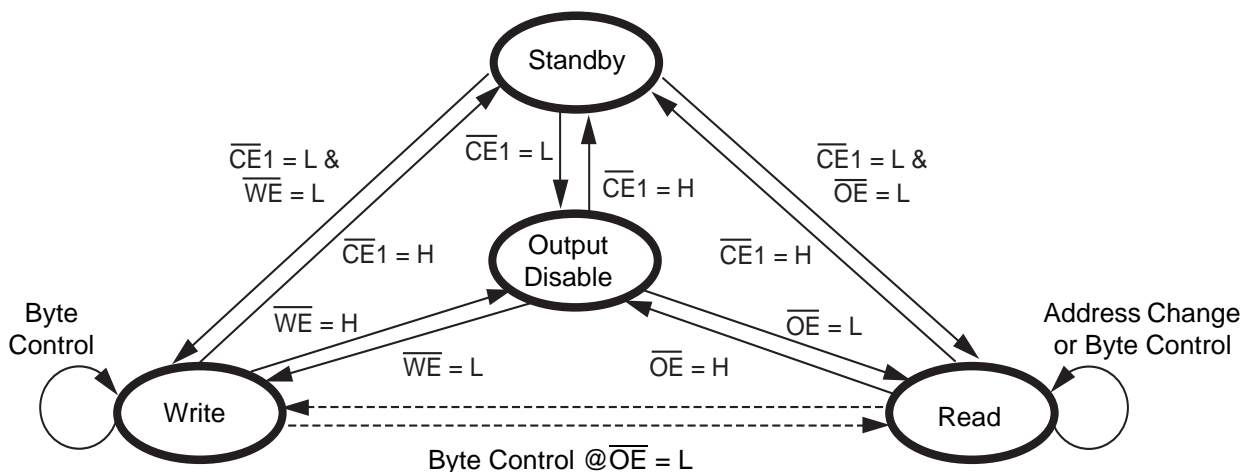
\*13 : WAIT output is driven in High level during burst write operation.

## STATE DIAGRAM

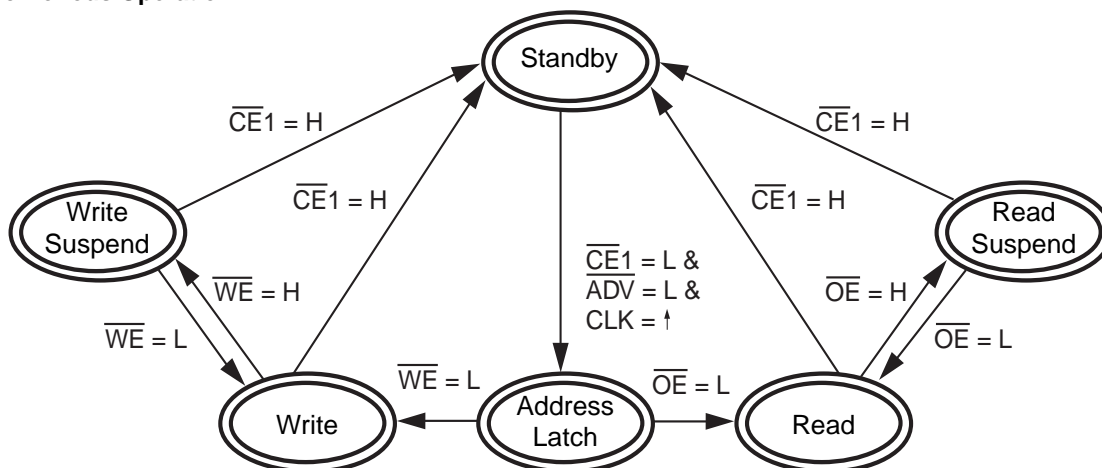
### Initial/Standby State



### Asynchronous Operation



### Synchronous Operation



\* : Assuming  $\overline{\text{WE}}$  Level Control

Note : Assuming all the parameters specified in AC CHARACTERISTICS are satisfied. Refer to the "FUNCTION TRUTH TABLE", "FUNCTIONAL DESCRIPTION", "2. AC Characteristics" in "ELECTRICAL CHARACTERISTICS", and "TIMING DIAGRAMS" for details.

## ■ FUNCTIONAL DESCRIPTION

This device supports asynchronous read & write operation and synchronous burst read and burst write operations for faster memory access and features four kinds of power down modes for power saving as user configurable option.

### • Power-up

It is required to follow the power-up timing to start executing proper device operation. Refer to "Power-up Timing". After Power-up, the device defaults to asynchronous read & write operation mode with sleep power down feature.

### • Configuration Register

The Configuration Register(CR) is used to configure the type of device function among optional features. Each selection of features is set through CR Set sequence after power-up. If CR Set sequence is not performed after power-up, the device is configured for asynchronous operations with sleep power down feature as default configuration. The content of CR can be confirmed using CR Verify sequence.

### • CR Set & Verify Sequence

The CR Set and CR Verify requires total 6 read/write operations with unique address and data. The device should be in standby mode in the interval between each read/write operation. The following table shows the detail sequence of CR Set and CR Verify.

Cycle #	Address	CR Set		CR Verify	
		Operation	Data	Operation	Data
1st	7FFFFFFh (MSB)	Read	Read Data (RDa)	Read	Read Data (RDa)
2nd	7FFFFFFh	Write	RDa	Write	RDa
3rd	7FFFFFFh	Write	RDa	Write	RDa
4th	7FFFFFFh	Write	CR Key 0	Write	CR Key 0
5th	7FFFFFFh	Write	CR Key 1	Read	CR Key 1
6th	7FFFFFFh	Write	CR Key 2	Read	CR Key 2

The 1st cycle is to read from most significant address(MSB).

The 2nd and 3rd cycles are to write to MSB. If the 2nd or 3rd cycle is written into the different address, the CR Set is cancelled and the data written by the 2nd or 3rd cycle is valid as a normal write operation. It is recommended to write back the data(RDa) read by 1st cycle to MSB in order to secure the data.

The 4th cycle is to write the appropriate "CR Key 0" to select the CR Set or CR Verify.

The 5th and 6th cycles are to access into MSB to set the "CR Keys" or to verify the "CR Keys". Refer to the "CR Key Table". If the 4th to 6th cycles are not access into MSB, the CR Set or CR Verify are cancelled and CR input or output data will be invalid.

Once this CR Set sequence is performed from an initial CR Set to the other new CR Set, the written data stored in the memory cell array may be lost. Therefore CR Set sequence should be performed prior to regular read/write operation if necessary to change from the default configuration.

## • CR Key Table

### CR Key 0

CR Key 0 should be set at 4th cycle of the CR Set or Verify sequence.

Pin Name	Register Name	Function	Key	Description	Note
DQ <sub>0</sub>	CRSV	CR Set/Verify	0	CR Verify	
			1	CR Set	
DQ <sub>7</sub> to DQ <sub>1</sub>	—	—	1	Reserved for future use	*1
DQ <sub>15</sub> to DQ <sub>8</sub>	—	—	1	Unused bits must be 1	*2

### CR Key 1

CR Key 1 should be set or read at 5th cycle of the CR Set or Verify sequence.

Pin Name	Register Name	Function	Key	Description	Note
DQ <sub>1</sub> , DQ <sub>0</sub>	PS	Partial Size	00	32M-bit Partial	*3
			01	16M-bit Partial	*3
			10	64M-bit Partial	*3
			11	Sleep [Default]	*3
DQ <sub>4</sub> to DQ <sub>2</sub>	BL	Burst Length	000, 001	Reserved for future use	*1
			010	8 words	
			011	16 words	
			100	32 words	
			101	64 words	
			110	128 words	
			111	Reserved for future use	*1
DQ <sub>5</sub>	M	Mode	0	Synchronous Mode (Burst Read/Write)	*4
			1	Asynchronous Mode [Default] (Random Read/Write)	*5
DQ <sub>7</sub> , DQ <sub>6</sub>	DS	Driver Size	00	+	
			01	Reserved for future use	*1
			10	–	
			11	Center [Default]	
DQ <sub>15</sub> to DQ <sub>8</sub>	—	—	1	Unused bits must be 1	*2



## CR Key 2

CR Key 2 should be set or read at 6th cycle of the CR Set or Verify sequence.

Pin Name	Register Name	Function	Key	Description	Note
DQ <sub>2</sub> to DQ <sub>0</sub>	RL	Read Latency	000, 001	Reserved for future use	*1
			010	4 clocks	
			011	5 clocks	
			100	6 clocks	
			101 to 111	Reserved for future use	*1
DQ <sub>3</sub>	—	—	1	Reserved for future use	*2
DQ <sub>4</sub>	—	—	0	Reserved for future use	*6
DQ <sub>5</sub>	—	—	1	Reserved for future use	*2
DQ <sub>6</sub>	RA	Reset to Asynchronous	0	Reset to Asynchronous mode	*7
			1	Remain the previous mode	*3
DQ <sub>7</sub>	WC	Write Control	0	$\overline{WE}$ Single Clock Pulse Control without Write Suspend Function	
			1	$\overline{WE}$ Level Control with Write Suspend Function	
DQ <sub>15</sub> to DQ <sub>8</sub>	—	—	1	Unused bits must be 1	*2

\*1 : It is prohibited to apply this key.

\*2 : Must be set to "1".

\*3 : Sleep and Partial power down mode are effective only when RA = 1.

\*4 : If M = 0, all the registers must be set with appropriate Key input at the same time.

\*5 : If M = 1, PS and DS must be set with appropriate Key input at the same time. Except for PS and DS, all the other key inputs must be "1".

\*6 : Must be set to "0".

\*7 : In case of RA = 0, CE2 brought to Low reset the device to asynchronous standby state regardless PS set value therefore Sleep and Partial power down mode are not available.

## • Power Down

The Power Down is low power idle state controlled by CE2. CE2 Low drives the device in power down mode and maintains low power idle state as long as CE2 is kept Low. CE2 High resumes the device from power down mode.

This device has four power down modes, Sleep, 16 M-bit Partial, 32 M-bit Partial, and 64 M-bit Partial. Those power down modes are effective when RA = 1. The selection of power down mode is set through CR Set sequence. Each mode has following data retention features.

Mode	Data Retention Size	Retention Address
Sleep [default]	No	N/A
16 M-bit Partial	16 M bits	000000h to 0FFFFFFh
32 M-bit Partial	32 M bits	000000h to 1FFFFFFh
64 M-bit Partial	64 M bits	000000h to 3FFFFFFh

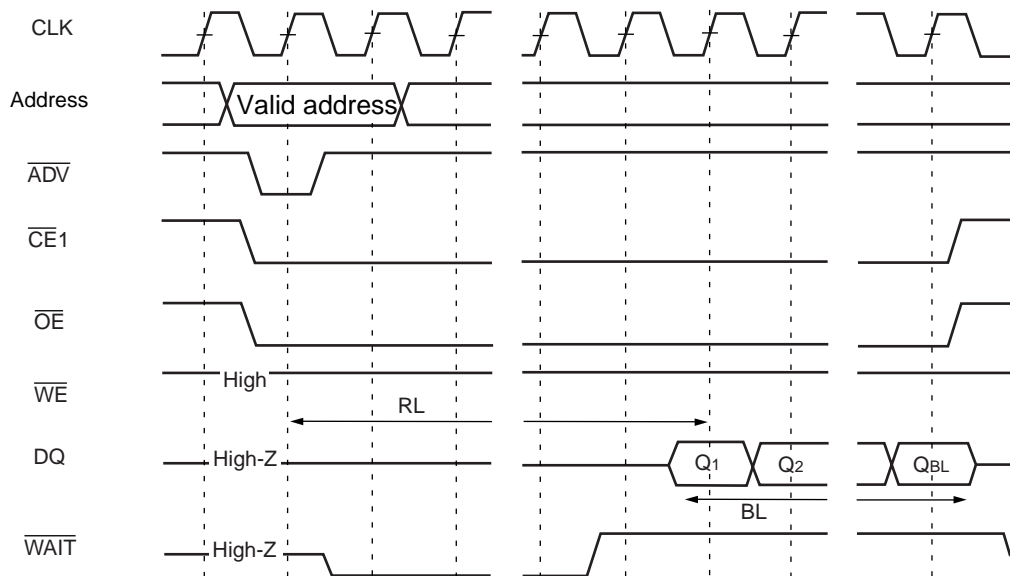
The default state is Sleep and it is the lowest power consumption. However all data will be lost once CE2 is brought to Low for Power Down. It is not required to perform CR Set sequence to set to Sleep mode after power-up in case of asynchronous operation.

When RA = 0, CE2 brought to Low reset the device to asynchronous standby state regardless PS set value.

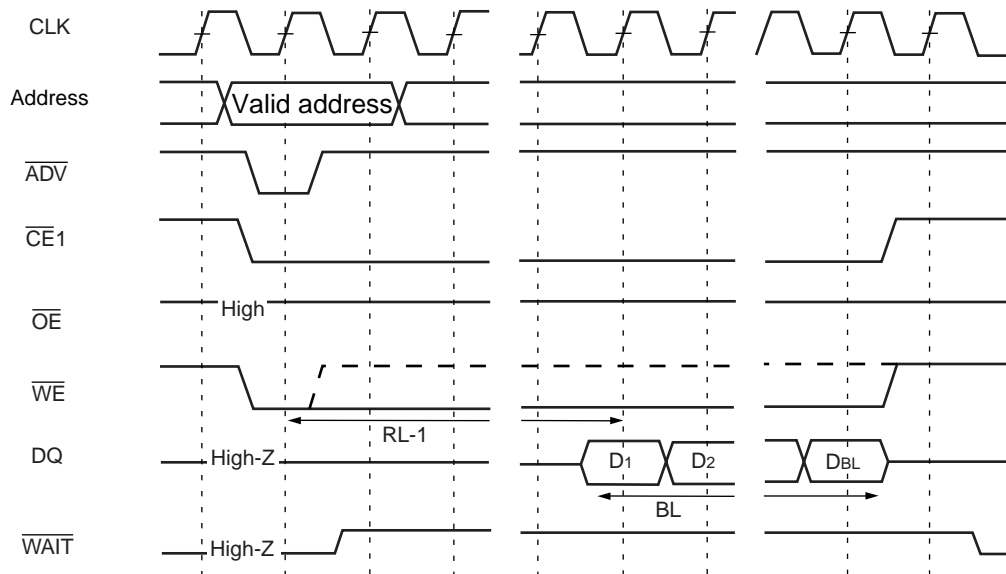
## • Burst Read/Write Operation

Synchronous burst read/write operation provides faster memory access that synchronized to the microcontroller or system bus frequency. Configuration Register(CR) Set is required to perform a burst read & write operation after power-up. Once CR Set sequence is performed to select the synchronous burst mode, the device is configured to synchronous burst read/write operation mode with corresponding RL and BL that is set through CR Set sequence together with the operation mode.

## • Burst Read Operation



## • Burst Write Operation



## • CLK Input Function

The CLK is input signal to synchronize the memory to the microcontroller or system bus frequency during synchronous burst read & write operation. The CLK input increments the device internal address counter and the valid edge of CLK is referred for latency counts from address latch, burst write data latch, and the burst read data output. During synchronous operation mode, CLK input must be supplied except for standby state and power down state. CLK is a “don't care” during asynchronous operation.

## • $\overline{\text{ADV}}$ Input Function

The  $\overline{\text{ADV}}$  is input signal to latch the valid address. It is applicable to the synchronous operation as well as asynchronous operation.  $\overline{\text{ADV}}$  input is active during  $\overline{\text{CE1}} = \text{L}$  and  $\overline{\text{CE1}} = \text{H}$  disables  $\overline{\text{ADV}}$  input.

During synchronous burst read/write operation,  $\overline{\text{ADV}} = \text{H}$  disables all address inputs. Once  $\overline{\text{ADV}}$  is brought to High after the valid address latch, it is inhibited to bring  $\overline{\text{ADV}}$  Low until the end of burst or until the burst operation is terminated.  $\overline{\text{ADV}}$  Low pulse is mandatory for the synchronous burst read/write operation mode to latch the valid address input.

During asynchronous operation,  $\overline{\text{ADV}} = \text{H}$  also disables all address inputs.  $\overline{\text{ADV}}$  can be tied to Low during asynchronous operations and it is not necessary to control  $\overline{\text{ADV}}$  to High.

## • $\overline{\text{WAIT}}$ Output Function

The  $\overline{\text{WAIT}}$  is output signal to indicate the data bus status when the device is operating in the synchronous burst mode.

During burst read operation,  $\overline{\text{WAIT}}$  output is enabled after specified time duration from  $\overline{\text{CE1}} = \text{L}$ .  $\overline{\text{WAIT}}$  output Low indicates data output at next clock cycle is invalid, and  $\overline{\text{WAIT}}$  output becomes High one clock cycle prior to valid data output. During  $\overline{\text{OE}}$  read suspend,  $\overline{\text{WAIT}}$  output doesn't indicate the data bus status but carries the same level from previous clock cycle (kept High).

During burst write operation,  $\overline{\text{WAIT}}$  output is enabled after specified time duration from  $\overline{\text{CE1}} = \text{L}$ .  $\overline{\text{WAIT}}$  output to High level after specified time duration from  $\overline{\text{WE}} = \text{L}$  or  $\overline{\text{CE1}} = \text{L}$  whichever occurs last and kept High for entire write cycles including  $\overline{\text{WE}}$  write suspend. The actual write data latching starts on the appropriate clock edge with respect to Read Latency, and Burst Length. During  $\overline{\text{WE}}$  write suspend,  $\overline{\text{WAIT}}$  output doesn't indicate the data bus status but carries the same level from previous clock cycle (kept High).

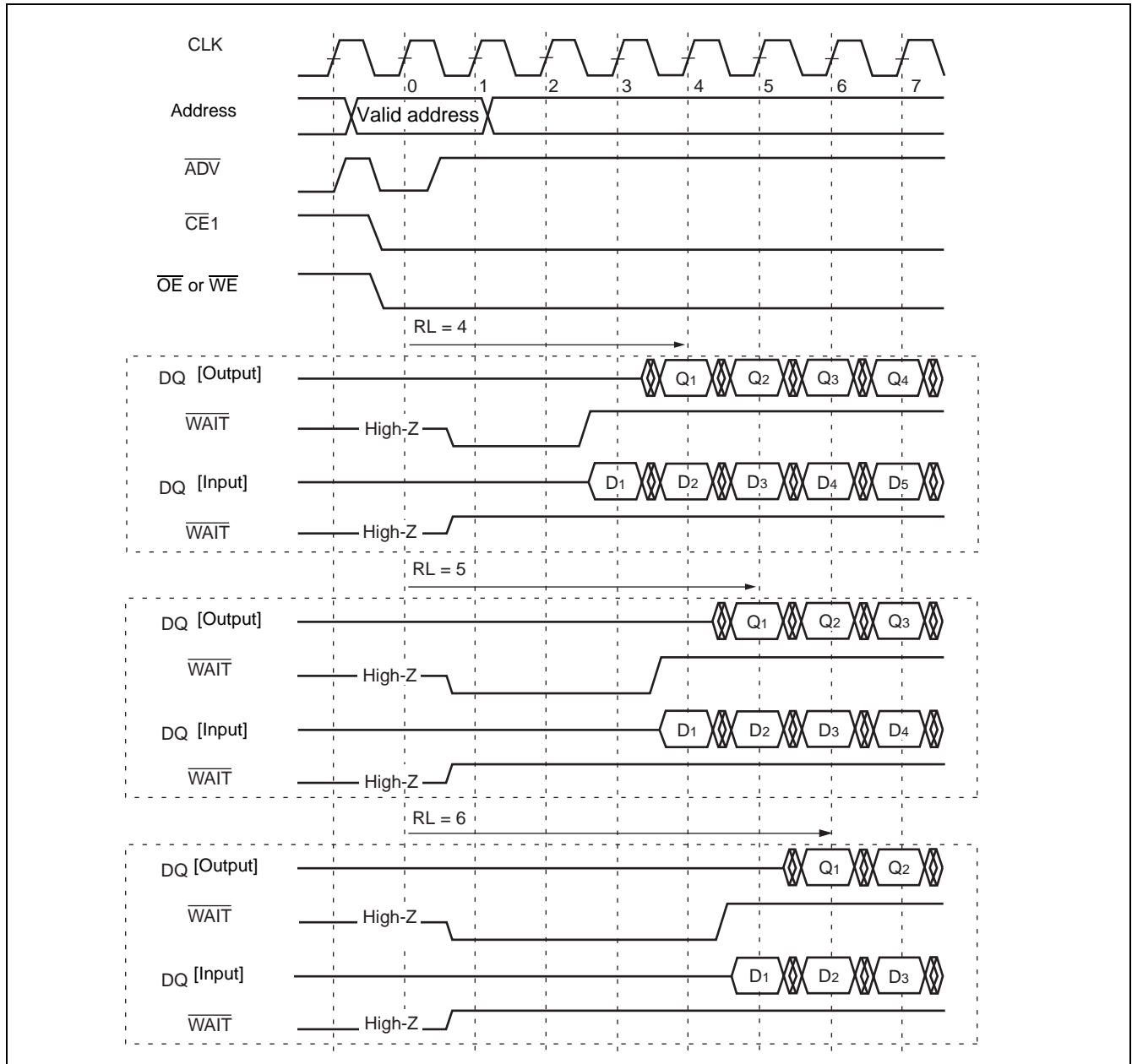
This device doesn't incur additional output delay against internal refresh operation. Therefore, the burst operation is always started after the fixed latency with respect to Read Latency. And there is no waiting cycle asserted in the middle of burst operation except for the burst read or write suspend by  $\overline{\text{OE}}$  brought to High or  $\overline{\text{WE}}$  brought to High. Thus, once  $\overline{\text{WAIT}}$  output is enabled and brought to High,  $\overline{\text{WAIT}}$  output keeps High level until the end of burst or until the burst operation is terminated.

When the device is operating in the asynchronous mode,  $\overline{\text{WAIT}}$  output is always in High Impedance.

## • Latency

Read Latency (RL) is the number of clock cycles between the address being latched and first read data becoming available during synchronous burst read operation. It is set through CR Set sequence after power-up. Once specific RL is set through CR Set sequence, write latency, that is the number of clock cycles between address being latched and first write data being latched, is automatically set to RL-1.

The burst operation is always started after the fixed latency with respect to Read Latency set in CR.



## • Address Latch by $\overline{ADV}$

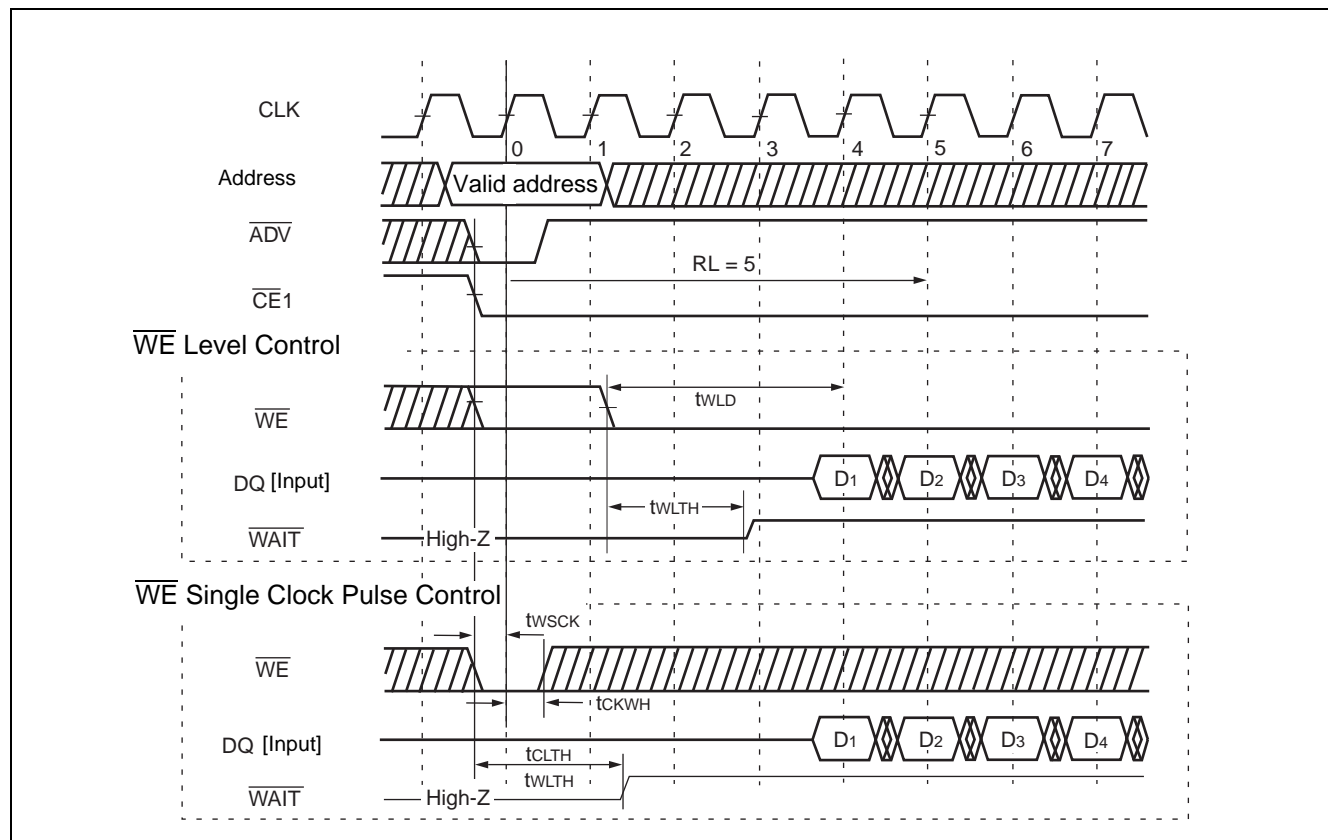
The  $\overline{ADV}$  latches the valid address presence on address inputs. During synchronous burst read/write operation mode, all the addresses are determined on first rising edge when  $\overline{ADV} = \overline{CE1} = L$ . The specified minimum value of  $\overline{ADV} = L$  setup time and hold time against valid edge of clock where RL count is begun must be satisfied for appropriate RL counts. Valid address must be determined with specified setup time against valid clock edge. And the determined valid address must not be changed during  $\overline{ADV} = L$  period.

## • Burst Length

Burst Length is the number of word to be read or written during synchronous burst read/write operation as the result of a single address latch cycle. It can be set on 8, 16, 32, 64, 128 words boundary for entire address through CR Set sequence. The burst type is sequential that is incremental decoding scheme within a boundary address. Starting from an initial address being latched, the device internal address counter assigns +1 to the previous address until reaching the end of boundary address and then wrap round to least significant address (= 0). After completing read data output or write data latch for the set burst length, operation automatically ended.

## • Write Control

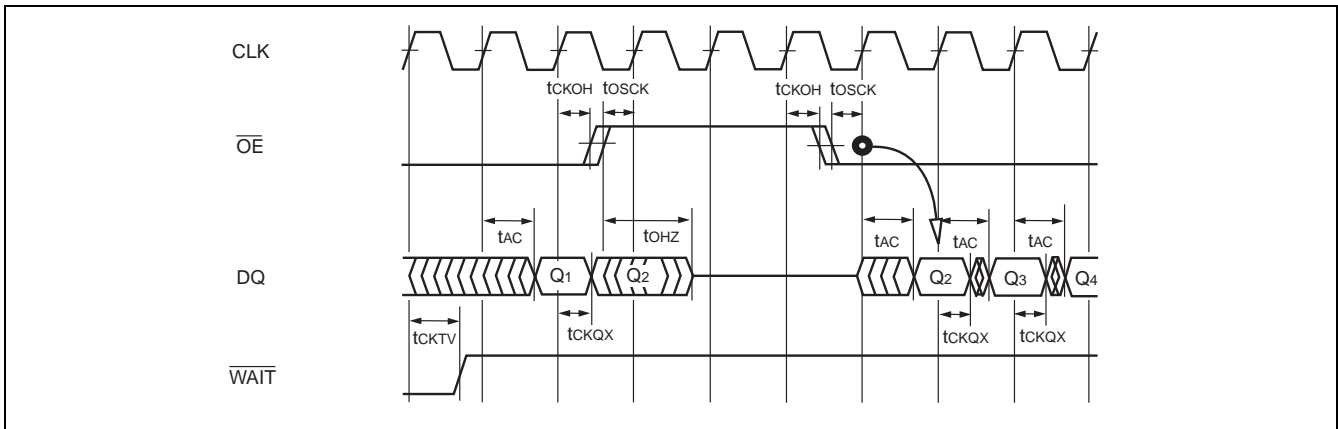
The device has two types of  $\overline{WE}$  signal control method, " $\overline{WE}$  Level Control" and " $\overline{WE}$  Single Clock Pulse Control", for synchronous burst write operation. It is configured through CR Set sequence. When device is operating in " $\overline{WE}$  Single Clock Pulse Control" mode, burst write operation is determined by  $\overline{WE} = L$  at the rising edge of CLK. In case of " $\overline{WE}$  Level Control",  $\overline{WE}$  can be High at address latching and  $\overline{WE} = L$  enables burst write operation.



## • Burst Read Suspend

Burst read operation can be suspended by  $\overline{OE}$  High pulse. During burst read operation,  $\overline{OE}$  brought to High suspends the burst read operation. Once  $\overline{OE}$  is brought to High with the specified setup time against clock where the data being suspended, the device internal counter is suspended, and the data output becomes high impedance after specified time duration. It is inhibited to suspend the first data output at the beginning of burst read.  $\overline{OE}$  brought to Low resumes the burst read operation. Once  $\overline{OE}$  is brought to Low, data output becomes valid after specified time duration, and the internal address counter is reactivated. The last data output being suspended as the result of  $\overline{OE} = H$  and first data output as the result of  $\overline{OE} = L$  are from the same address.

In order to guarantee to output last data before suspension and first data after resumption, the specified minimum value of  $\overline{OE} = L$  hold time and setup time against clock edge must be satisfied respectively.



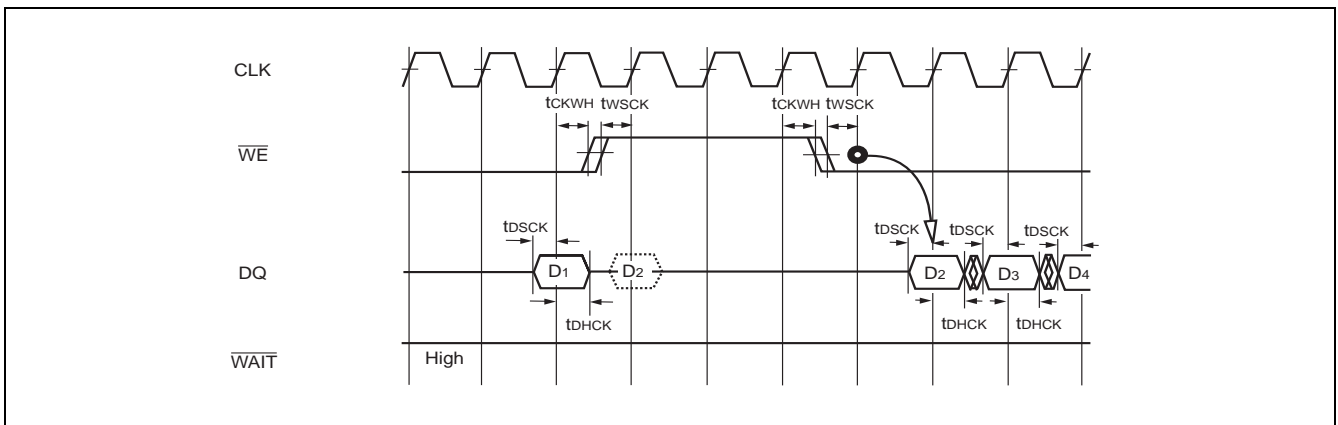
## • Burst Write Suspend

Burst write operation can be suspended by  $\overline{WE}$  High pulse. During burst write operation,  $\overline{WE}$  brought to High suspends the burst write operation. Once  $\overline{WE}$  is brought to High with the specified setup time against clock where the data being suspended, the device internal counter is suspended, data input is ignored. It is inhibited to suspend the first data input at the beginning of burst write.

$\overline{WE}$  brought to Low resumes the burst write operations. Once  $\overline{WE}$  is brought to Low, data input becomes valid after specified time duration, and the internal address counter is reactivated. The write address of the cycle where data being suspended and the first write address as the result of  $\overline{WE} = L$  are the same address.

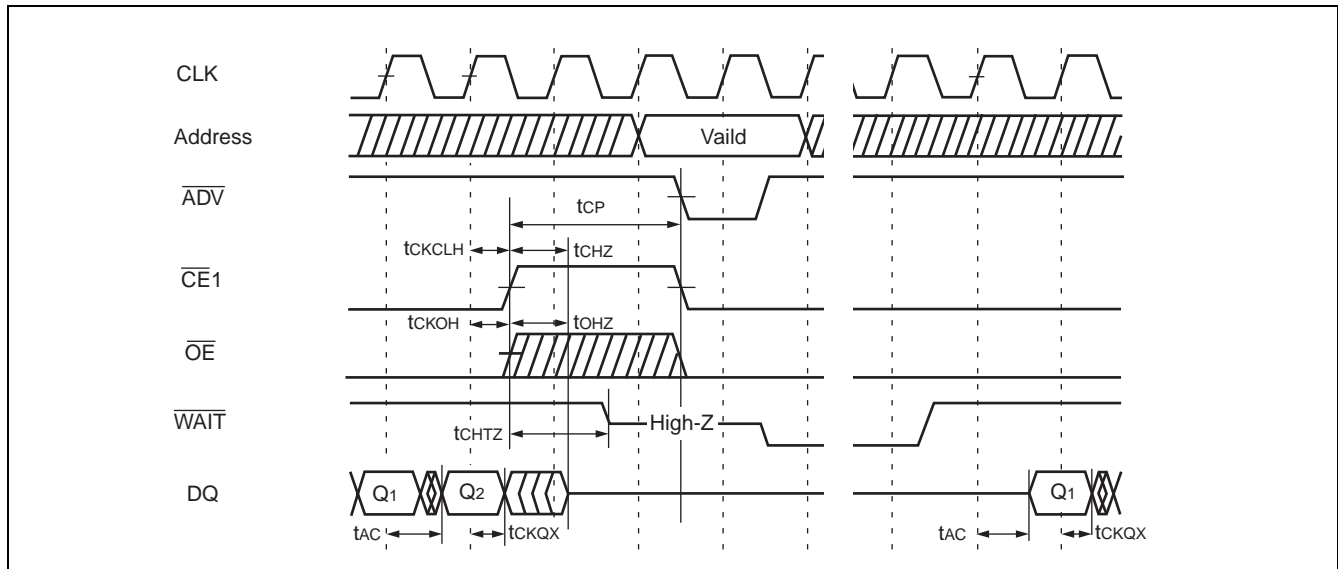
In order to guarantee to latch the last data input before suspension and first data input after resumption, the specified minimum value of  $\overline{WE} = L$  hold time and setup time against clock edge must be satisfied respectively.

Burst write suspend function is available only when the device is operating in  $\overline{WE}$  level controlled burst write.



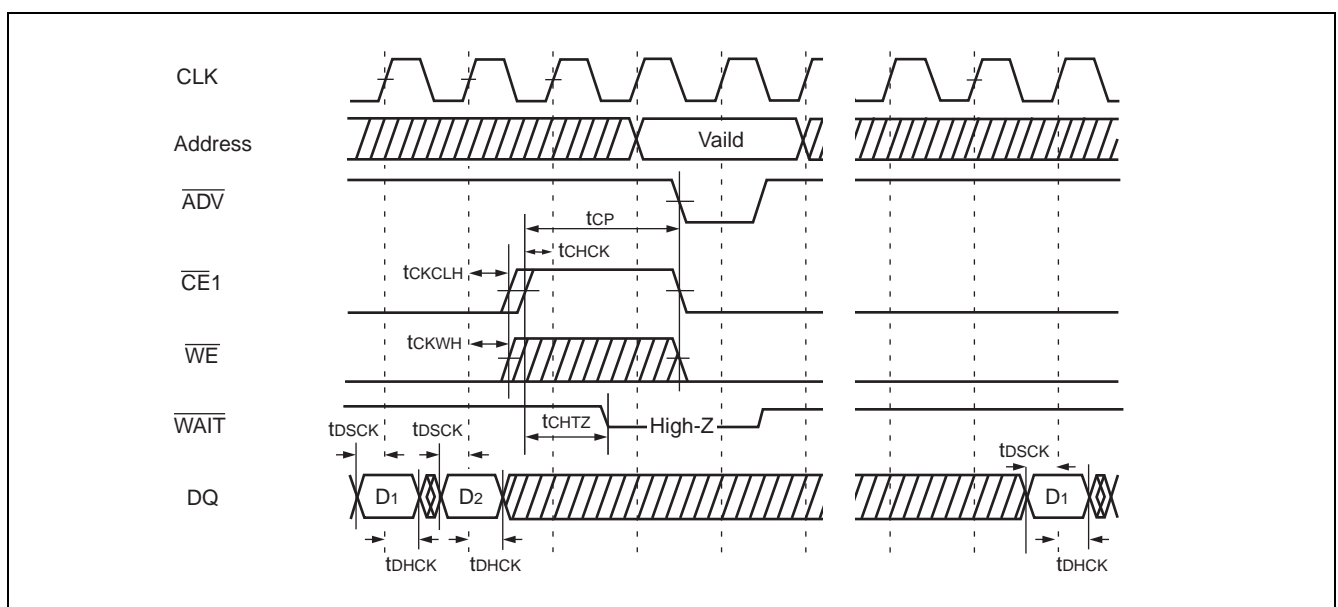
## • Burst Read Termination

Burst read operation can be terminated by  $\overline{CE1}$  brought to High. It is inhibited to terminate the burst read before first data output is completed. In order to guarantee last data output, the specified minimum value of  $\overline{CE1} = L$  hold time from the clock edge must be satisfied. After termination, the specified minimum recovery time is required to start a new access.



## • Burst Write Termination

Burst write operation can be terminated by  $\overline{CE1}$  brought to High. It is inhibited to terminate the burst write before first data input is completed. In order to guarantee last write data being latched, the specified minimum values of  $\overline{CE1} = L$  hold time from the clock edge must be satisfied. After termination, the specified minimum recovery time is required to start a new access.





## ■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Voltage of $V_{DD}$ Supply Relative to $V_{SS}$ *	$V_{DD}$	- 0.5	+ 2.3	V
Voltage at Any Pin Relative to $V_{SS}$ *	$V_{IN}$ , $V_{OUT}$	- 0.5	+ 2.3	V
Short Circuit Output Current	$I_{OUT}$	- 50	+ 50	mA
Storage Temperature	$T_{STG}$	- 55	+ 125	°C

\* : All voltages are referenced to  $V_{SS} = 0$  V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## ■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value		Unit
		Min	Max	
Power Supply Voltage*1	$V_{DD}$	1.7	1.95	V
Ground	$V_{SS}$	0	0	V
High Level Input Voltage*1, *2	$V_{IH}$	$V_{DD} \times 0.8$	$V_{DD} + 0.2$	V
Low Level Input Voltage*1, *3	$V_{IL}$	- 0.3	$V_{DD} \times 0.2$	V
Ambient Temperature	$T_A$	0	+ 70	°C

\*1 : All voltages are referenced to  $V_{SS} = 0$  V.

\*2 : Maximum DC voltage on input and I/O pins is  $V_{DD} + 0.2$  V. During voltage transitions, inputs may overshoot to  $V_{DD} + 1.0$  V for the periods of up to 5 ns.

\*3 : Minimum DC voltage on input and I/O pins is -0.3 V. During voltage transitions, inputs may undershoot  $V_{SS}$  to -1.0 V for the periods of up to 5 ns.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges.

Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

## ■ PIN CAPACITANCE

( $f = 1$  MHz,  $T_A = +25$  °C)

Parameter	Symbol	Test conditions	Value			Unit
			Min	Typ	Max	
Address Input Capacitance	$C_{IN1}$	$V_{IN} = 0$ V	—	—	5	pF
Control Input Capacitance	$C_{IN2}$	$V_{IN} = 0$ V	—	—	5	pF
Data Input/Output Capacitance	$C_{IO}$	$V_{IO} = 0$ V	—	—	8	pF

## ■ ELECTRICAL CHARACTERISTICS

### 1. DC Characteristics

(At recommended operating conditions unless otherwise noted)

Parameter	Symbol	Test Conditions		Value		Unit
				Min	Max	
Input Leakage Current	$I_{LI}$	$V_{SS} \leq V_{IN} \leq V_{DD}$		- 1.0	+ 1.0	$\mu A$
Output Leakage Current	$I_{LO}$	$0 V \leq V_{OUT} \leq V_{DD}$ , Output Disable		- 1.0	+ 1.0	$\mu A$
Output High Voltage Level	$V_{OH}$	$V_{DD} = V_{DD} (\text{Min})$ , $I_{OH} = - 0.5 \text{ mA}$		1.4	—	V
Output Low Voltage Level	$V_{OL}$	$I_{OL} = 1 \text{ mA}$		—	0.4	V
$V_{DD}$ Power Down Current	$I_{DDPS}$		Sleep	—	10	$\mu A$
	$I_{DDP16}$	$V_{DD} = V_{DD} (\text{Max})$ , $V_{IN} = V_{DD} \text{ or } V_{SS}$ , $\overline{CE2} = V_{SS}$	16 M-bit Partial	—	230	$\mu A$
	$I_{DDP32}$		32 M-bit Partial	—	260	$\mu A$
	$I_{DDP64}$		64 M-bit Partial	—	310	$\mu A$
$V_{DD}$ Standby Current	$I_{DDS}$	$V_{DD} = V_{DD} (\text{Max})$ , $V_{IN} (\text{including CLK}) = V_{IH} \text{ or } V_{IL}$ , $\overline{CE1} = \overline{CE2} = V_{IH}$		—	1.5	mA
	$I_{DDS1}$	$V_{DD} = V_{DD} (\text{Max})$ , $V_{IN} (\text{including CLK}) = V_{DD} \text{ or } V_{SS}$ , $\overline{CE1} = \overline{CE2} = V_{DD}$	$T_A \leq + 70 \text{ }^\circ\text{C}$	—	400	$\mu A$
			$T_A \leq + 40 \text{ }^\circ\text{C}$	—	200	$\mu A$
$V_{DD}$ Active Current	$I_{DDA1}$	$V_{DD} = V_{DD} (\text{Max})$ , $V_{IN} = V_{IH} \text{ or } V_{IL}$ , $\overline{CE1} = V_{IL} \text{ and } \overline{CE2} = V_{IH}$ , $I_{OUT} = 0 \text{ mA}$	$t_{RC}/t_{WC} = \text{Min}$	—	35	mA
	$I_{DDA2}$		$t_{RC}/t_{WC} = 1 \text{ } \mu\text{s}$	—	5	mA
$V_{DD}$ Burst Access Current	$I_{DDA4}$	$V_{DD} = V_{DD} (\text{Max})$ , $V_{IN} = V_{IH} \text{ or } V_{IL}$ , $\overline{CE1} = V_{IL} \text{ and } \overline{CE2} = V_{IH}$ , $t_{CK} = t_{CK} (\text{Min})$ , $BL = 128$ , $I_{OUT} = 0 \text{ mA}$		—	24	mA

Notes : • All voltages are referenced to  $V_{SS} = 0 \text{ V}$ .

- $I_{DD}$  depends on the output termination, load conditions, and AC characteristics.
- After power on, initialization following power-up timing is required. DC characteristics are guaranteed after the initialization.
- $I_{DDP16}$ ,  $I_{DDP32}$ ,  $I_{DDP64}$ ,  $I_{DDS}$  and  $I_{DDS1}$  might be higher for up to 400 ms after power-up or power down/standby mode entry.

## 2. AC Characteristics

### (1) Asynchronous Read Operation

(At recommended operating conditions unless otherwise noted)

Parameter	Symbol	Value		Unit	Notes
		Min	Max		
Read Cycle Time	$t_{RC}$	70	1000	ns	*1, *2
$\overline{CE1}$ Access Time	$t_{CE}$	—	70	ns	*3
$\overline{OE}$ Access Time	$t_{OE}$	—	40	ns	*3
Address Access Time	$t_{AA}$	—	70	ns	*3, *4
$\overline{ADV}$ Access Time	$t_{AV}$	—	70	ns	*3
$\overline{LB}$ , $\overline{UB}$ Access Time	$t_{BA}$	—	30	ns	*3
Output Data Hold Time	$t_{OH}$	3	—	ns	*3
$\overline{CE1}$ Low to Output Low-Z	$t_{CLZ}$	10	—	ns	*5
$\overline{OE}$ Low to Output Low-Z	$t_{OLZ}$	10	—	ns	*5
$\overline{LB}$ , $\overline{UB}$ Low to Output Low-Z	$t_{BLZ}$	10	—	ns	*5
$\overline{CE1}$ High to Output High-Z	$t_{CHZ}$	—	9.5	ns	*3
$\overline{OE}$ High to Output High-Z	$t_{OHZ}$	—	9.5	ns	*3
$\overline{LB}$ , $\overline{UB}$ High to Output High-Z	$t_{BHZ}$	—	9.5	ns	*3
Address Setup Time to $\overline{ADV}$ Low	$t_{ASVL}$	– 5	—	ns	*6
Address Setup Time to $\overline{CE1}$ Low	$t_{ASC}$	– 5	—	ns	*6
Address Setup Time to $\overline{OE}$ Low	$t_{ASO}$	0	—	ns	
$\overline{ADV}$ Low Pulse Width	$t_{VPL}$	7	—	ns	*6
$\overline{ADV}$ High Pulse Width	$t_{VPH}$	10	—	ns	
Address Hold Time from $\overline{ADV}$ High	$t_{AHV}$	5	—	ns	
Address Invalid Time	$t_{AX}$	—	10	ns	*4, *7
Address Hold Time from $\overline{CE1}$ High	$t_{CHAH}$	– 5	—	ns	*8
Address Hold Time from $\overline{OE}$ High	$t_{OHAH}$	– 5	—	ns	
$\overline{WE}$ High to $\overline{OE}$ Low Time for Read	$t_{WHOL}$	10	1000	ns	*9
$\overline{CE1}$ High Pulse Width	$t_{CP}$	10	—	ns	

\*1 : Maximum value is applicable if  $\overline{CE1}$  is kept at Low without change of address input.

\*2 : Address should not be changed within a minimum  $t_{RC}$ .

\*3 : The output load 50 pF with 50  $\Omega$  termination to  $V_{DD} \times 0.5$  V.

\*4 : Applicable when  $\overline{CE1}$  is kept at Low.

\*5 : The output load 5 pF without any other load.

\*6 :  $t_{VPL}$  is specified from the falling edge of either  $\overline{CE1}$  or  $\overline{ADV}$  whichever comes late. The sum of actual  $t_{VPL}$  and  $t_{ASVL}$  (or  $t_{ASC}$ ) must be equal or greater than the specified minimum value of  $t_{VPL}$ .

\*7 : Applicable to address access when at least two of address inputs are switched from the previous state.

\*8 :  $t_{RC}$  (Min) must be satisfied.

\*9 : If actual value of  $t_{WHOL}$  is shorter than specified minimum values, the actual  $t_{AA}$  of following Read may become longer by the amount of subtracting actual value from specified minimum value.

## (2) Asynchronous Write Operation

(At recommended operating conditions unless otherwise noted)

Parameter	Symbol	Value		Unit	Notes
		Min	Max		
Write Cycle Time	$t_{WC}$	70	1000	ns	*1, *2
Address Setup Time to $\overline{ADV}$ Low	$t_{ASVL}$	- 5	—	ns	*3
Address Setup Time	$t_{AS}$	0	—	ns	
$\overline{ADV}$ Low Pulse Width	$t_{VPL}$	7	—	ns	*3
$\overline{ADV}$ High Pulse Width	$t_{VPH}$	10	—	ns	
Address Hold Time from $\overline{ADV}$ High	$t_{AHV}$	5	—	ns	
$\overline{CE1}$ Write Pulse Width	$t_{CW}$	45	—	ns	*2, *4
$\overline{WE}$ Write Pulse Width	$t_{WP}$	45	—	ns	*2, *4
$\overline{LB}$ , $\overline{UB}$ Write Pulse Width	$t_{BW}$	45	—	ns	*2, *4
$\overline{LB}$ , $\overline{UB}$ Byte Mask Setup Time	$t_{BS}$	- 5	—	ns	*5
$\overline{LB}$ , $\overline{UB}$ Byte Mask Hold Time	$t_{BH}$	- 5	—	ns	*6
Write Recovery Time	$t_{WR}$	0	—	ns	*2, *7
$\overline{CE1}$ High Pulse Width	$t_{CP}$	10	—	ns	
$\overline{WE}$ High Pulse Width	$t_{WHP}$	10	1000	ns	*8
$\overline{LB}$ , $\overline{UB}$ High Pulse Width	$t_{BHP}$	10	1000	ns	*8
Data Setup Time	$t_{DS}$	15	—	ns	
Data Hold Time	$t_{DH}$	0	—	ns	
$\overline{OE}$ High to $\overline{CE1}$ Low Setup Time for Write	$t_{OHCL}$	- 5	—	ns	*9
$\overline{OE}$ High to Address Setup Time for Write	$t_{OES}$	0	—	ns	*10

\*1 : Maximum value is applicable if  $\overline{CE1}$  is kept at Low without any address change.

\*2 : The sum of write pulse width ( $t_{CW}$ ,  $t_{WP}$  or  $t_{BW}$ ) and actual write recovery time ( $t_{WR}$ ) must be equal or greater than specified minimum  $t_{WC}$ .

\*3 :  $t_{VPL}$  is specified from the falling edge of either  $\overline{CE1}$  or  $\overline{ADV}$  whichever comes late. The sum of actual  $t_{VPL}$  and  $t_{ASVL}$  must be equal or greater than the specified minimum value of  $t_{VPL}$ .

\*4 : Write pulse width is defined from High to Low transition of  $\overline{CE1}$ ,  $\overline{WE}$ ,  $\overline{LB}$ , or  $\overline{UB}$ , whichever occurs last.

\*5 : Applicable for byte mask only. Byte mask setup time is defined to the High to Low transition of  $\overline{CE1}$  or  $\overline{WE}$  whichever occurs last.

\*6 : Applicable for byte mask only. Byte mask hold time is defined from the Low to High transition of  $\overline{CE1}$  or  $\overline{WE}$  whichever occurs first.

\*7 : Write recovery time is defined from Low to High transition of  $\overline{CE1}$ ,  $\overline{WE}$ ,  $\overline{LB}$ , or  $\overline{UB}$ , whichever occurs first.

\*8 : Maximum specification of  $t_{WHP}$  and  $t_{BHP}$  are applicable to Output Disable mode when  $\overline{CE} = L$ ,  $\overline{WE} = \overline{OE} = H$  after write operation. Refer to “(7) Asynchronous Write Timing 2 ( $\overline{WE}$  Control)” in “■ TIMING DIAGRAMS”.

\*9 : If  $\overline{OE}$  is Low after minimum  $t_{OHCL}$ , read cycle is initiated. In other word,  $\overline{OE}$  must be brought to High within 5 ns after  $\overline{CE1}$  is brought to Low.

\*10 : If  $\overline{OE}$  is Low after a new address input, read cycle is initiated. In other word,  $\overline{OE}$  must be brought to High at the same time or before a new address becomes valid.

### (3) Synchronous Operation - Clock Input (Burst Mode)

(At recommended operating conditions unless otherwise noted)

Parameter		Symbol	Value		Unit	Notes
			Min	Max		
Clock Period	RL = 6	t <sub>CK</sub>	13	—	ns	*1
	RL = 5		15	—	ns	*1
	RL = 4		18	—	ns	*1
Clock High Time		t <sub>CKH</sub>	3	—	ns	
Clock Low Time		t <sub>CKL</sub>	3	—	ns	
Clock Transition Time		t <sub>CKT</sub>	—	1.5	ns	*2

\*1 : Clock period is defined between valid clock edges.

\*2 : Clock transition time is defined between V<sub>IH</sub> (Min) and V<sub>IL</sub> (Max)

### (4) Synchronous Operation - Address Latch (Burst Mode)

(At recommended operating conditions unless otherwise noted)

Parameter		Symbol	Value		Unit	Notes
			Min	Max		
Address Setup Time to CLK		t <sub>ASCK</sub>	3	—	ns	*1
Address Hold Time from CLK		t <sub>CKAH</sub>	1	—	ns	*1
$\overline{\text{ADV}}$ Low Pulse Width		t <sub>VPL</sub>	7	—	ns	*2
$\overline{\text{ADV}}$ Low Setup Time to CLK	RL = 6	t <sub>VSCK</sub>	3	—	ns	*1
	RL = 4, 5		5	—		
$\overline{\text{CE1}}$ Low Setup Time to CLK	RL = 6	t <sub>CLCK</sub>	3	—	ns	*1
	RL = 4, 5		5	—		
$\overline{\text{ADV}}$ Low Hold Time from CLK		t <sub>CKVH</sub>	1	—	ns	*1
$\overline{\text{CE1}}$ High Hold Time from CLK		t <sub>CKCH</sub>	1	—	ns	*3

\*1 : Applicable to the 1st rising clock edge.

\*2 : t<sub>VPL</sub> is specified from the falling edge of either  $\overline{\text{CE1}}$  or  $\overline{\text{ADV}}$  whichever comes late.

\*3 : Applicable to the positive clock edge before address latching.

## (5) Synchronous Read Operation (Burst Mode)

(At recommended operating conditions unless otherwise noted)

Parameter	Symbol	Value		Unit	Notes
		Min	Max		
Burst Read Cycle Time	$t_{RCB}$	—	8000	ns	
CLK Access Time	RL = 6	—	6	ns	*1
	RL = 4, 5	—	9	ns	*1
Output Hold Time from CLK	$t_{CKQX}$	2	—	ns	*1
$\overline{CE}1$ Low to $\overline{WAIT}$ Low	$t_{CLTL}$	5	15	ns	*1
CLK to $\overline{WAIT}$ Valid Time	$t_{CKTV}$	—	6	ns	*1
$\overline{WAIT}$ Valid Hold Time from CLK	$t_{CKTX}$	2	—	ns	*1
$\overline{CE}1$ Low to Output Low-Z	$t_{CLZ}$	10	—	ns	*2
$\overline{OE}$ Low to Output Low-Z	$t_{OLZ}$	10	—	ns	*2, *3
$\overline{LB}$ , $\overline{UB}$ Low to Output Low-Z	$t_{BLZ}$	10	—	ns	*2
$\overline{CE}1$ High to Output High-Z	$t_{CHZ}$	—	9.5	ns	*1
$\overline{OE}$ High to Output High-Z	$t_{OHZ}$	—	9.5	ns	*1
$\overline{LB}$ , $\overline{UB}$ High to Output High-Z	$t_{BHZ}$	—	9.5	ns	*1
$\overline{CE}1$ High to $\overline{WAIT}$ High-Z	$t_{CHTZ}$	—	9.5	ns	*1
$\overline{OE}$ Low Setup Time to 1st Data-output	$t_{OLQ}$	34	—	ns	
$\overline{LB}$ , $\overline{UB}$ Setup Time to 1st Data-output	$t_{BLQ}$	26	—	ns	*4
$\overline{OE}$ Setup Time to CLK	$t_{OSCK}$	3	—	ns	
$\overline{OE}$ Hold Time from CLK	$t_{CKOH}$	1	—	ns	
Burst End $\overline{CE}1$ Low Hold Time from CLK	$t_{CKCLH}$	1	—	ns	
$\overline{LB}$ , $\overline{UB}$ Hold Time from CLK	$t_{CKBH}$	1	—	ns	
$\overline{CE}1$ High Pulse Width	$t_{CP}$	9.5	—	ns	

\*1 : The output load 50 pF with 50  $\Omega$  termination to  $V_{DD} \times 0.5$  V.

\*2 : The output load 5 pF without any other load.

\*3 :  $t_{OLZ}$  must not be applied after burst read suspend.

\*4 : Once  $\overline{LB}$ ,  $\overline{UB}$  are determined,  $\overline{LB}$ ,  $\overline{UB}$  must not be changed until the end of burst read.

## (6) Synchronous Write Operation (Burst Mode)

(At recommended operating conditions unless otherwise noted)

Parameter	Symbol	Value		Unit	Notes
		Min	Max		
Burst Write Cycle Time	$t_{WCB}$	—	8000	ns	
Data Setup Time to CLK	$t_{DSCK}$	3	—	ns	
Data Hold Time from CLK	$t_{DHCK}$	1	—	ns	
$\overline{WE}$ Low Setup Time to 1st Data Input	$t_{WLD}$	45	—	ns	
$\overline{WE}$ Setup Time to CLK	$t_{WSCK}$	3	—	ns	
$\overline{WE}$ Hold Time from CLK	$t_{CKWH}$	1	—	ns	
$\overline{LB}$ , $\overline{UB}$ Setup Time to CLK	$t_{BSCK}$	3	—	ns	*1
$\overline{LB}$ , $\overline{UB}$ Hold Time from CLK	$t_{CKBH}$	1	—	ns	*1
$\overline{CE1}$ Low to $\overline{WAIT}$ High	$t_{CLTH}$	5	15	ns	*2, *3
$\overline{WE}$ Low to $\overline{WAIT}$ High	$t_{WLTH}$	—	15	ns	*2, *3
$\overline{CE1}$ High to $\overline{WAIT}$ High-Z	$t_{CHTZ}$	—	9.5	ns	*2
Burst End $\overline{CE1}$ Low Hold Time from CLK	$t_{CKCLH}$	1	—	ns	
Burst End $\overline{CE1}$ High Setup Time to next CLK	$t_{CHCK}$	3	—	ns	
$\overline{CE1}$ High Pulse Width	$t_{CP}$	9.5	—	ns	

\*1 :  $t_{BSCK}$  and  $t_{CKBH}$  should be satisfied for byte mask control.

\*2 : The output load 50 pF with 50  $\Omega$  termination to  $V_{DD} \times 0.5$  V.

\*3 :  $\overline{WAIT}$  outputs Low-Z after  $t_{CLTH}$  (Min) from  $\overline{CE1} = L$ .  $\overline{WAIT}$  outputs to High level after  $t_{WLTH}$  or  $t_{CLTH}$  from  $\overline{WE} = L$  or  $\overline{CE1} = L$  whichever occurs last.

## (7) Power Down Parameters

(At recommended operating conditions unless otherwise noted)

Parameter	Symbol	Value		Unit	Notes
		Min	Max		
CE2 Low Setup Time for Power Down Entry	t <sub>CSP</sub>	10	—	ns	
CE2 Low Hold Time after Power Down Entry	t <sub>C2LP</sub>	70	—	ns	
CE2 Low Hold Time for Reset to Asynchronous Mode	t <sub>C2LPR</sub>	70	—	ns	*1
$\overline{\text{CE}}1$ High Hold Time following CE2 High after Power Down Exit [Sleep mode only]	t <sub>CHH</sub>	300	—	μs	*2
$\overline{\text{CE}}1$ High Hold Time following CE2 High after Power Down Exit [not in Sleep mode]	t <sub>CHHP</sub>	70	—	ns	*3
$\overline{\text{CE}}1$ High Setup Time following CE2 High after Power Down Exit	t <sub>CHS</sub>	0	—	ns	*2

\*1 : Applicable when RA = 0 (Reset to Asynchronous mode) .

\*2 : Applicable also to power-up.

\*3 : Applicable when Partial Power Down mode and Reset to Asynchronous mode are set.

## (8) Other Timing Parameters

(At recommended operating conditions unless otherwise noted)

Parameter	Symbol	Value		Unit	Notes
		Min	Max		
$\overline{\text{CE}}1$ High to $\overline{\text{OE}}$ Invalid Time for Standby Entry	t <sub>CHOX</sub>	0	—	ns	
$\overline{\text{CE}}1$ High to $\overline{\text{WE}}$ Invalid Time for Standby Entry	t <sub>CHWX</sub>	0	—	ns	*1
CE2 Low Hold Time after Power-up	t <sub>C2LH</sub>	50	—	μs	
$\overline{\text{CE}}1$ High Hold Time following CE2 High after Power-up	t <sub>CHH</sub>	300	—	μs	
Input Transition Time (except for CLK)	t <sub>tr</sub>	1	25	ns	*2, *3

\*1 : Some data might be written into any address location if t<sub>CHWX</sub> (Min) is not satisfied.

\*2 : Except for the CLK input transition time.

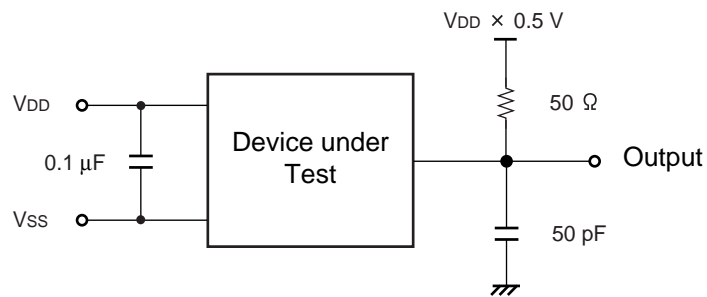
\*3 : The Input Transition Time (t<sub>tr</sub>) at AC testing is 3 ns for Asynchronous operation and 1.5 ns for Synchronous operation respectively. If actual t<sub>tr</sub> is longer than 3 ns or 1.5 ns specified as AC test condition, it may violate AC specification of some timing parameters. Refer to " (9) AC Test Conditions".



## (9) AC Test Conditions

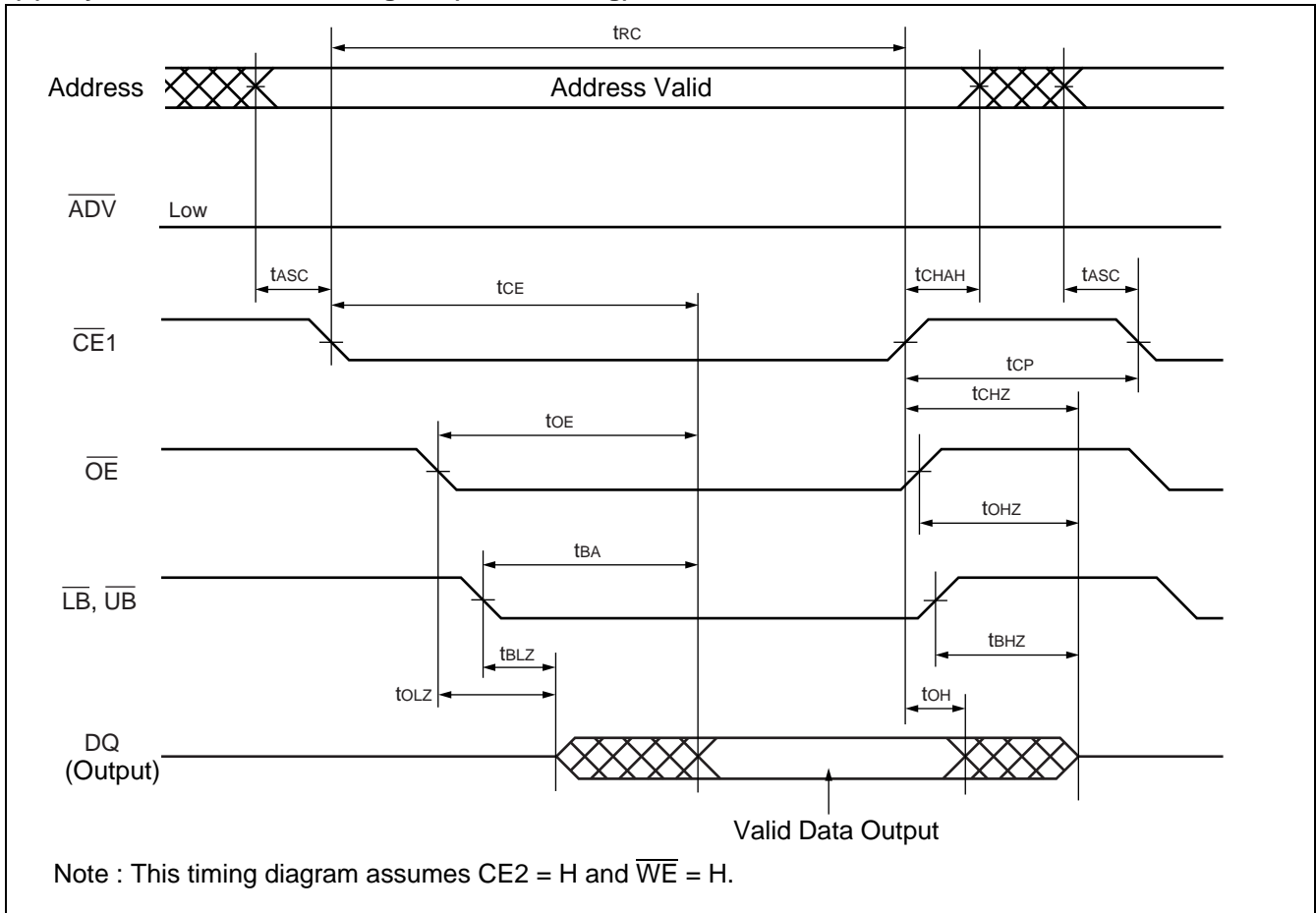
Description		Symbol	Test Setup	Value	Unit	Notes
Input High Level		$V_{IH}$	—	$V_{DD} \times 0.8$	V	
Input Low Level		$V_{IL}$	—	$V_{DD} \times 0.2$	V	
Input Timing Measurement Level		$V_{REF}$	—	$V_{DD} \times 0.5$	V	
Input Transition Time	Async.	$t_T$	Between $V_{IL}$ and $V_{IH}$	3	ns	
	Sync.			1.5	ns	

### • AC MEASUREMENT OUTPUT LOAD CIRCUIT

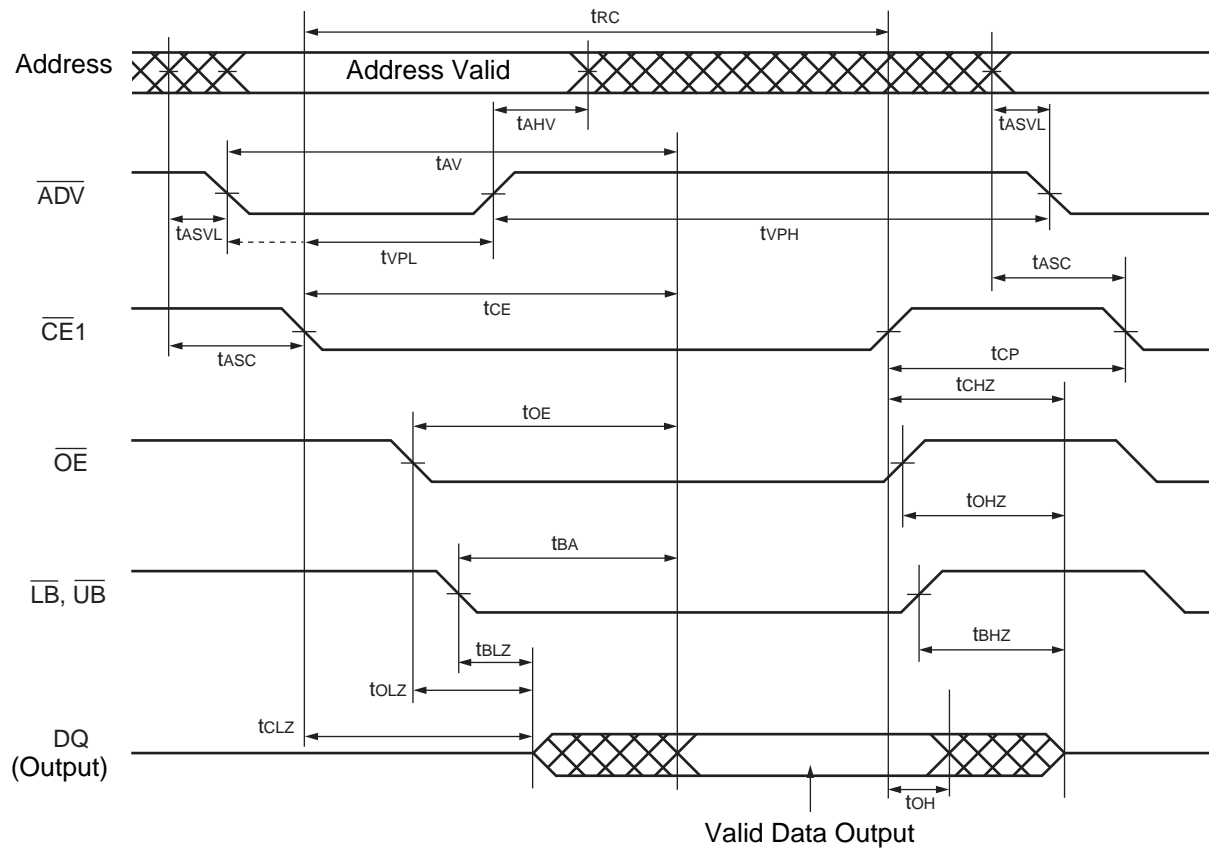


## ■ TIMING DIAGRAMS

### (1) Asynchronous Read Timing 1-1 (Basic Timing)

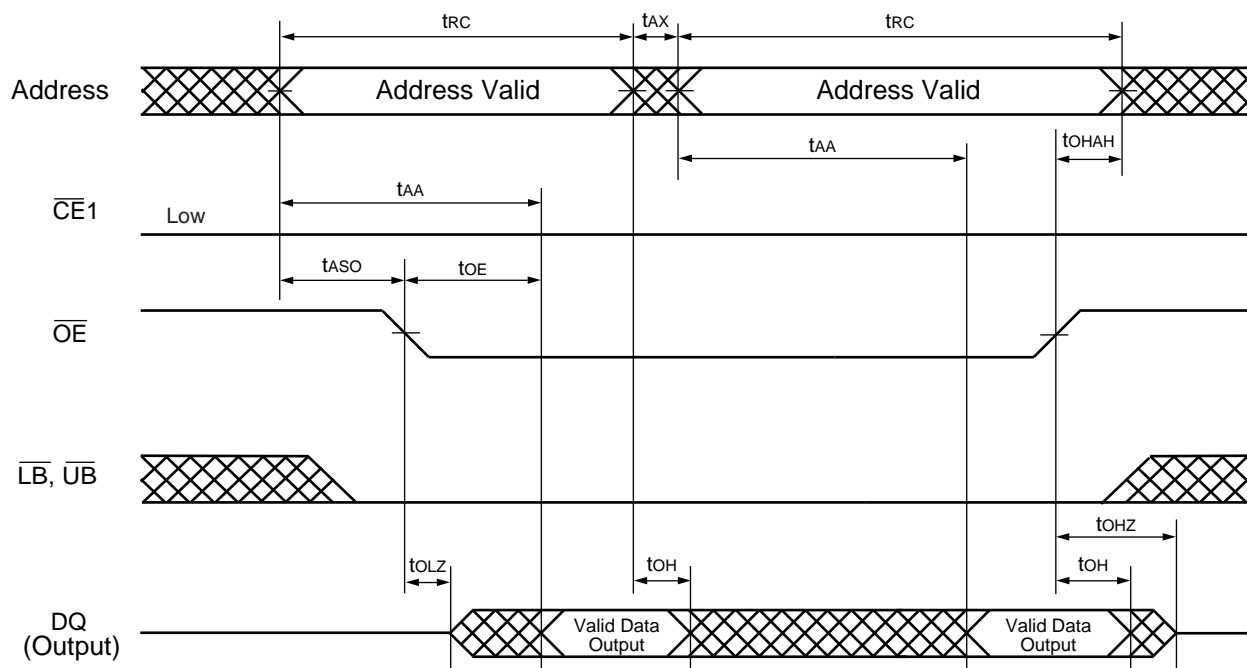


## (2) Asynchronous Read Timing 1-2 (Basic Timing)



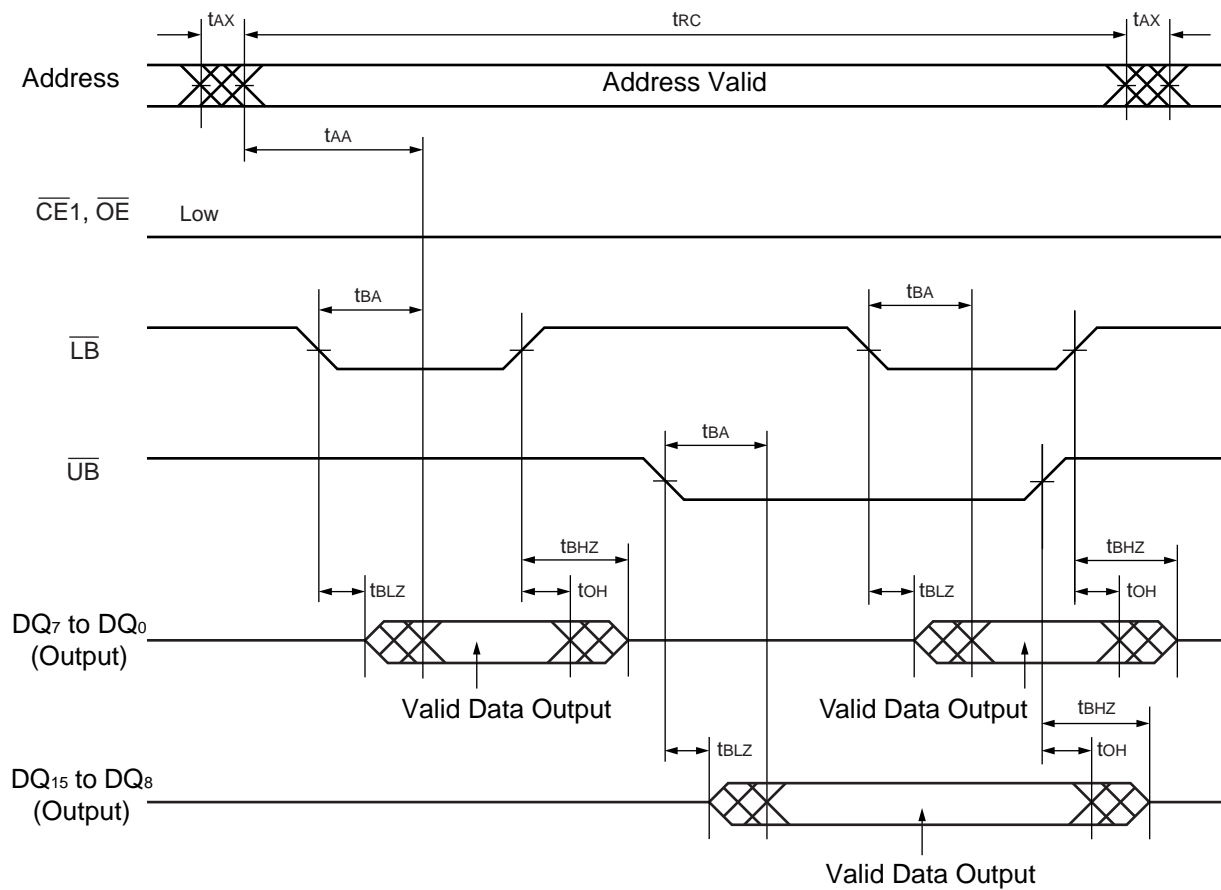
Note : This timing diagram assumes  $CE2 = H$  and  $\overline{WE} = H$ .

## (3) Asynchronous Read Timing 2 ( $\overline{OE}$ Control & Address Access)



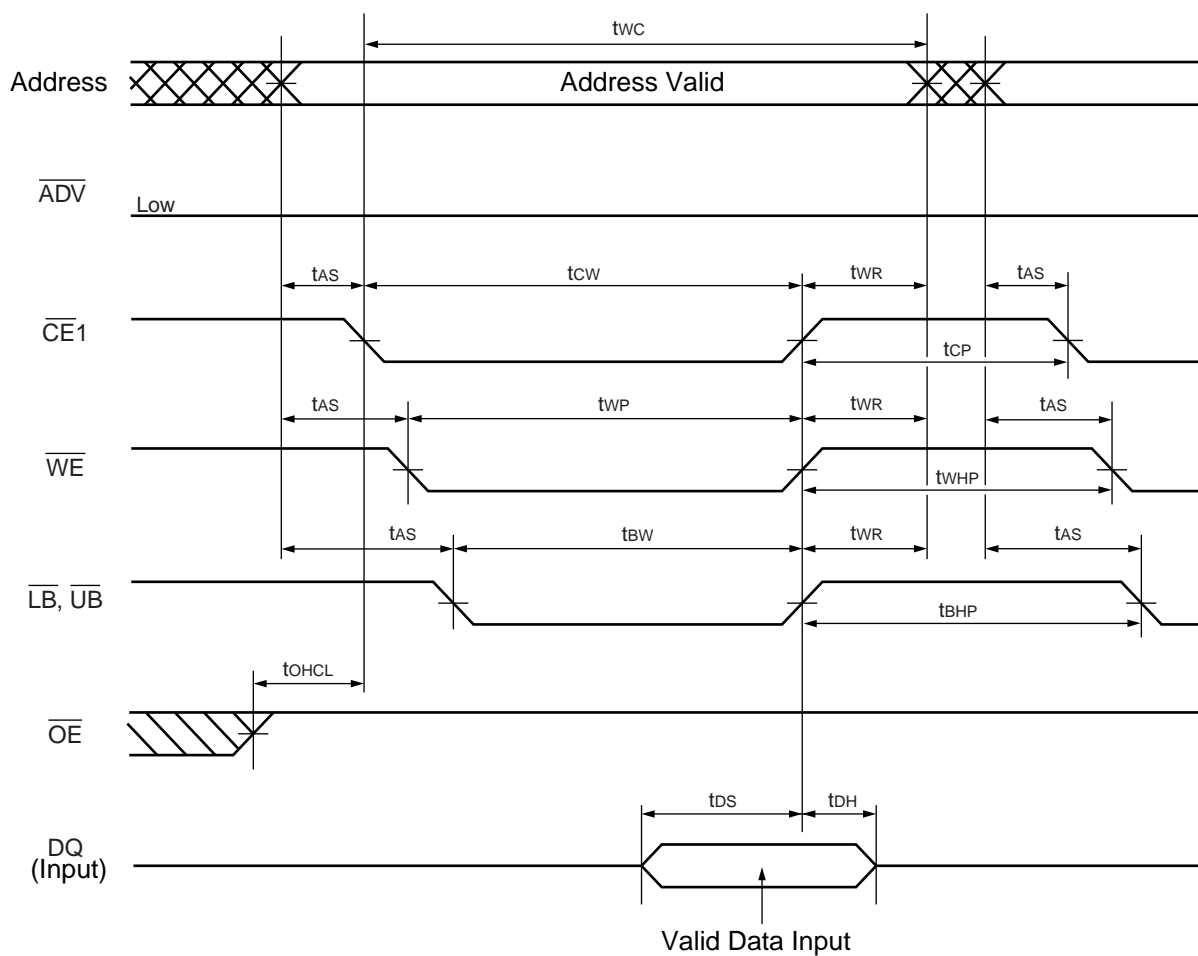
Note : This timing diagram assumes  $CE2 = H$ ,  $\overline{ADV} = L$  and  $\overline{WE} = H$ .

## (4) Asynchronous Read Timing 3 ( $\overline{\text{LB}}$ , $\overline{\text{UB}}$ Byte Control Access)



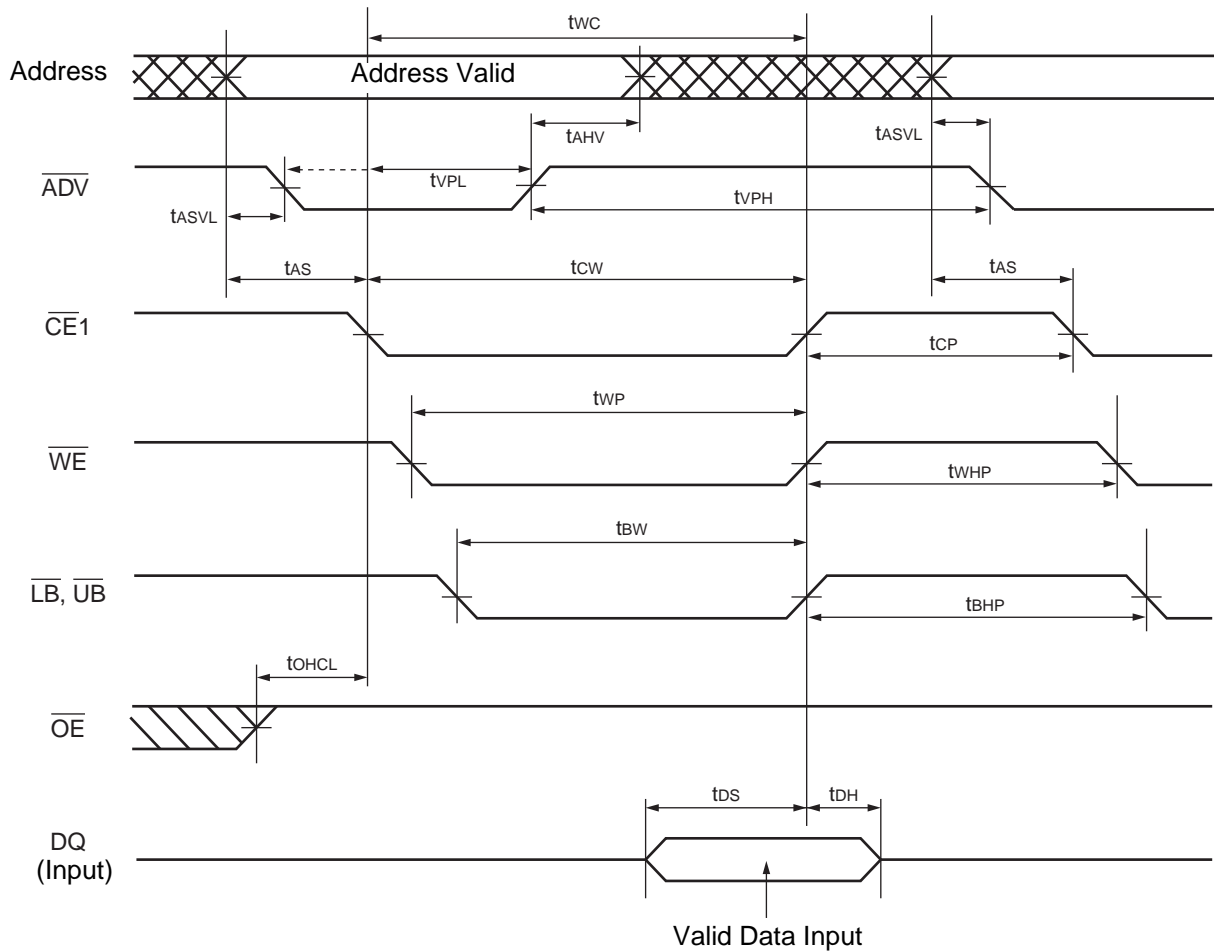
Note : This timing diagram assumes  $\text{CE2} = \text{H}$ ,  $\overline{\text{ADV}} = \text{L}$  and  $\overline{\text{WE}} = \text{H}$ .

## (5) Asynchronous Write Timing 1-1 (Basic Timing)



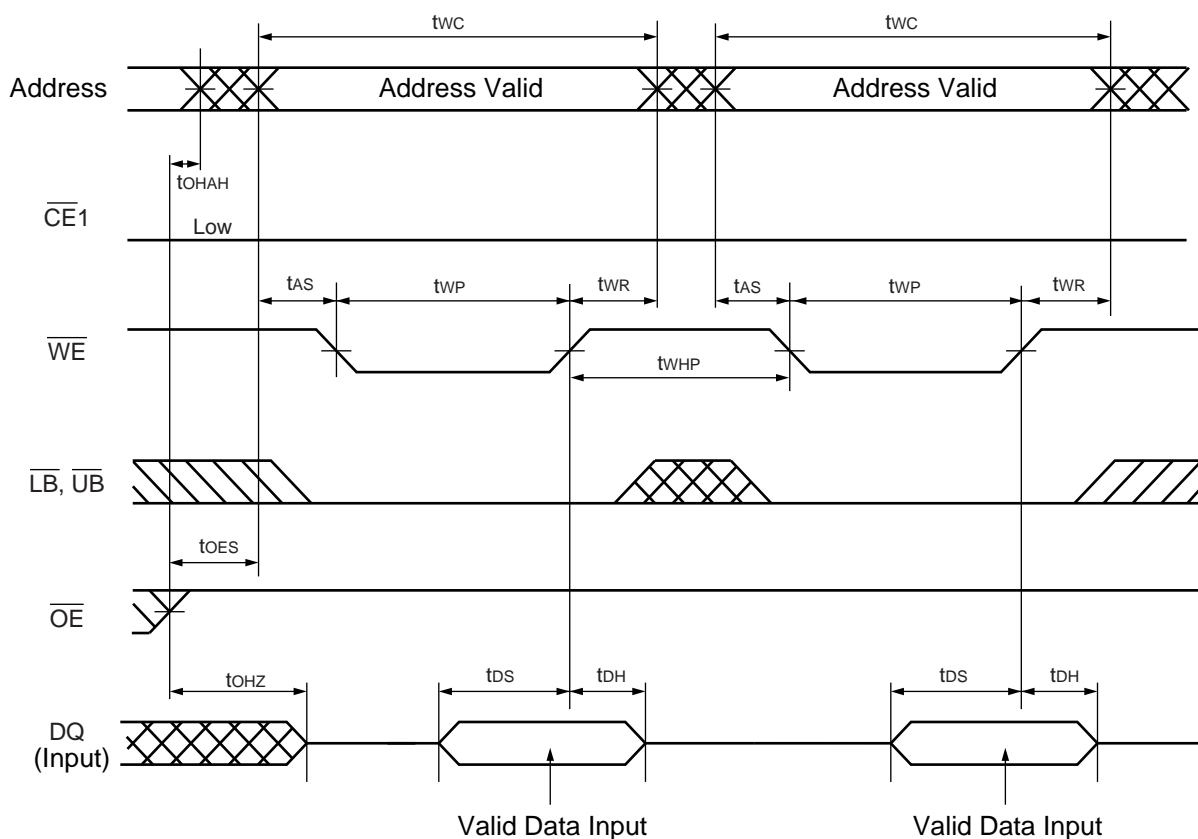
Note : This timing diagram assumes CE2 = H.

## (6) Asynchronous Write Timing 1-2 (Basic Timing)



Note : This timing diagram assumes CE2 = H.

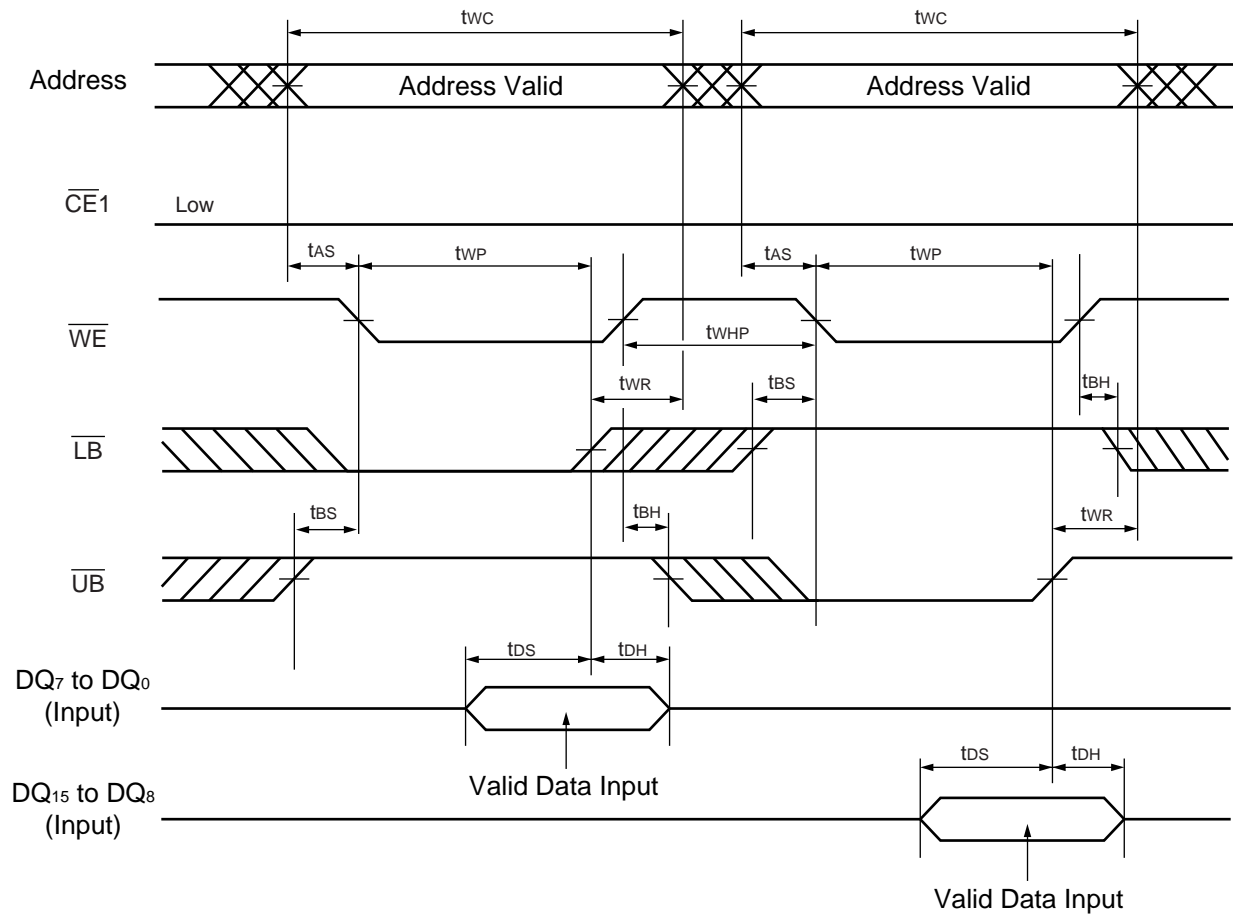
## (7) Asynchronous Write Timing 2 ( $\overline{\text{WE}}$ Control)



Note : This timing diagram assumes  $\text{CE2} = \text{H}$  and  $\overline{\text{ADV}} = \text{L}$ .

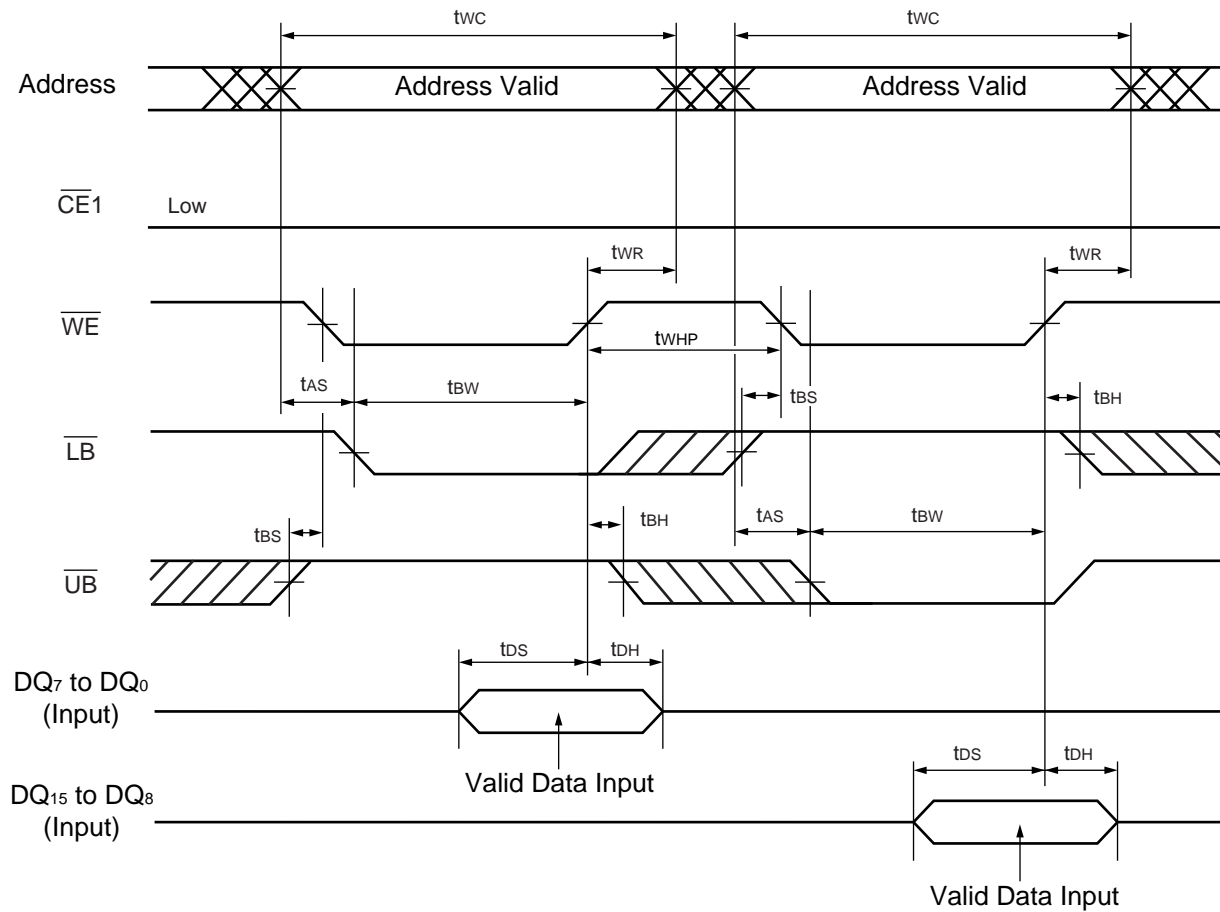


## (8) Asynchronous Write Timing 3-1 ( $\overline{WE}$ , $\overline{LB}$ , $\overline{UB}$ Byte Write Control)



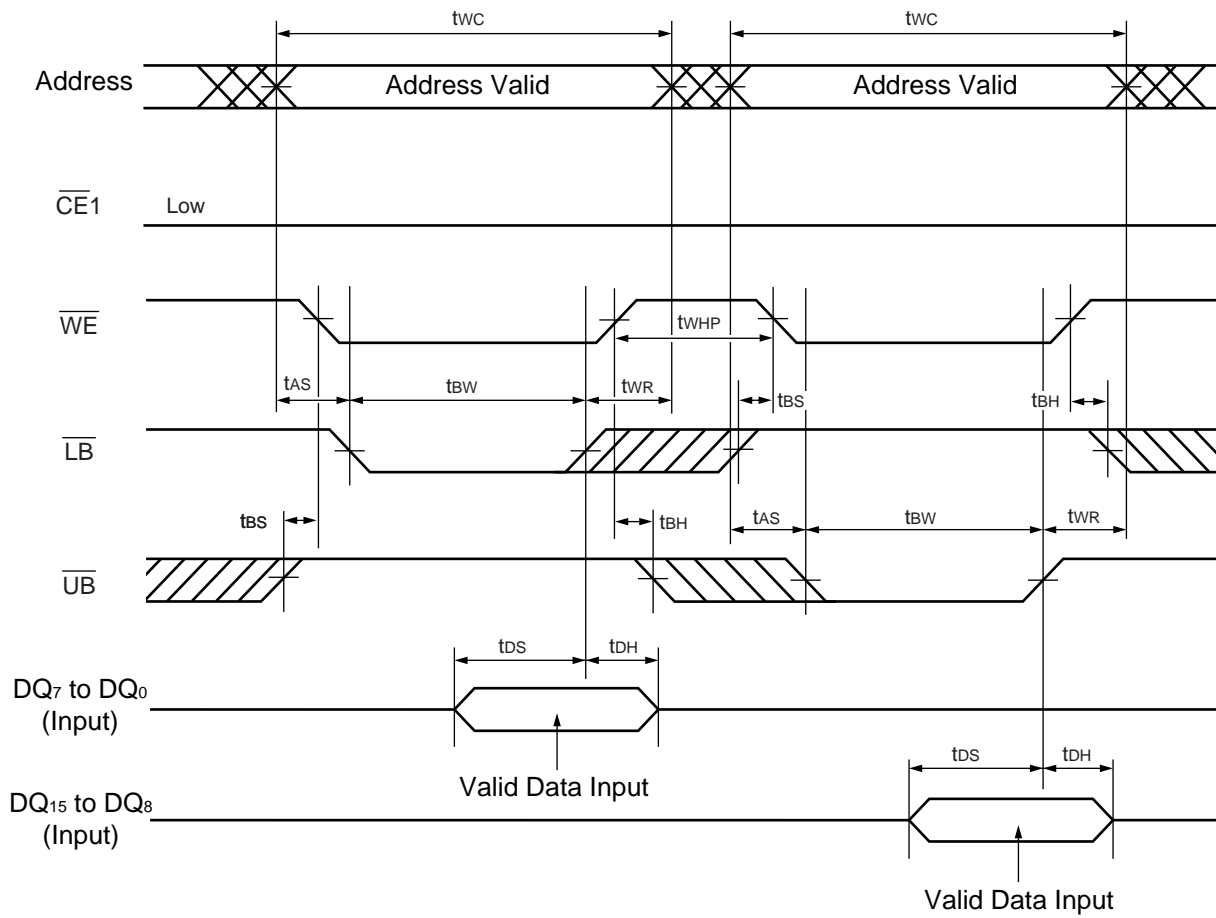
Note : This timing diagram assumes  $CE2 = H$ ,  $\overline{ADV} = L$  and  $\overline{OE} = H$ .

## (9) Asynchronous Write Timing 3-2 ( $\overline{WE}$ , $\overline{LB}$ , $\overline{UB}$ Byte Write Control)



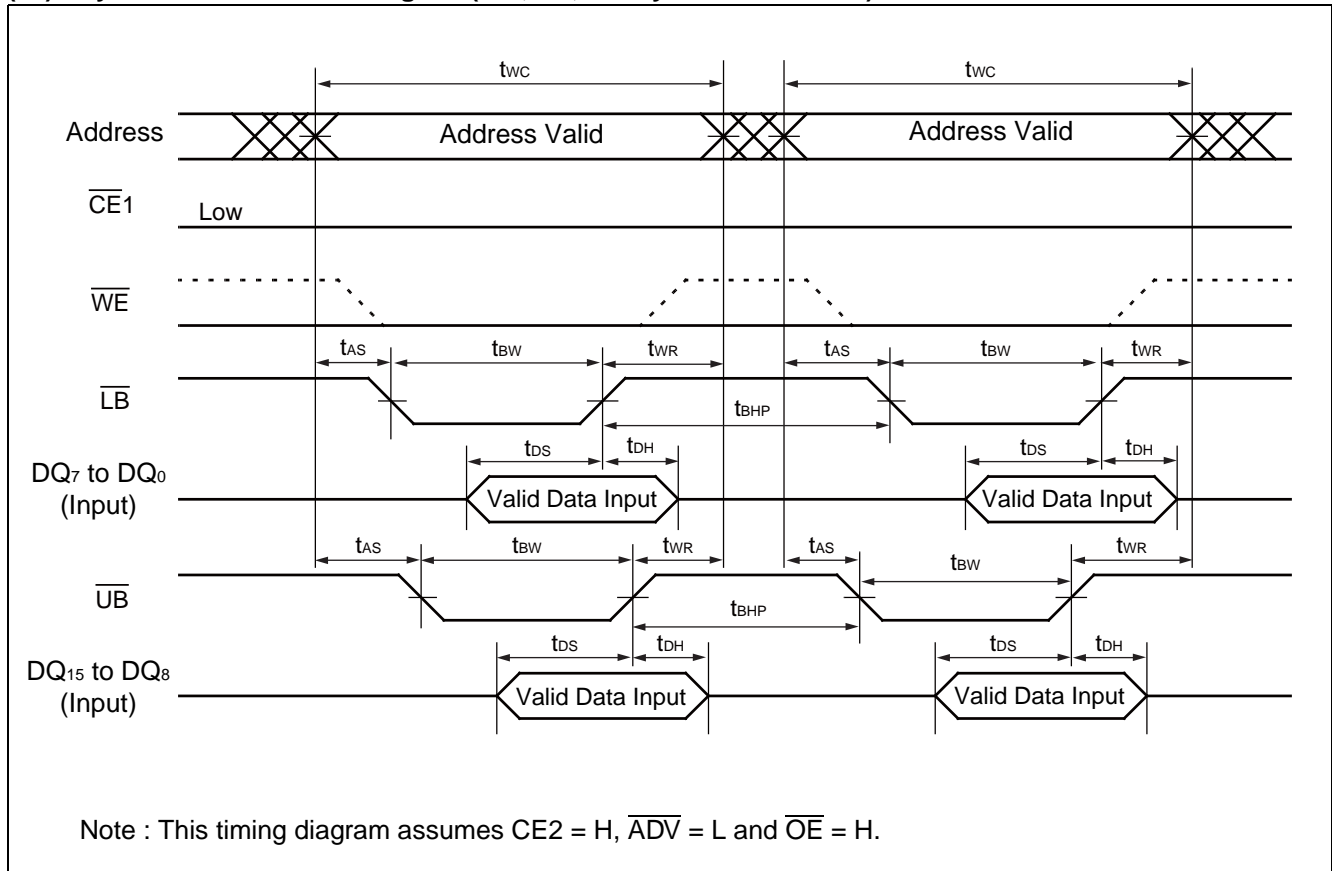
Note : This timing diagram assumes  $CE2 = H$ ,  $\overline{ADV} = L$  and  $\overline{OE} = H$ .

## (10) Asynchronous Write Timing 3-3 ( $\overline{WE}$ , $\overline{LB}$ , $\overline{UB}$ Byte Write Control)

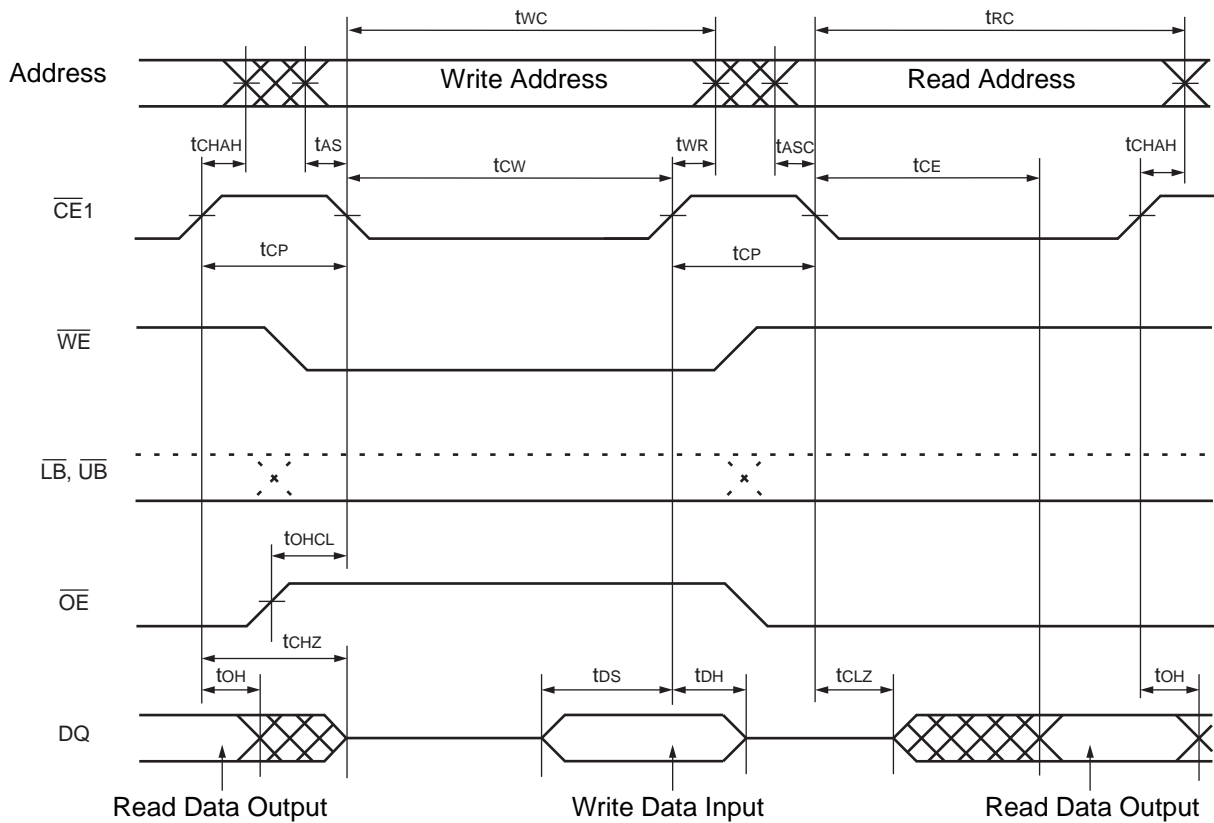


Note : This timing diagram assumes  $CE2 = H$ ,  $\overline{ADV} = L$  and  $\overline{OE} = H$ .

## (11) Asynchronous Write Timing 3-4 ( $\overline{WE}$ , $\overline{LB}$ , $\overline{UB}$ Byte Write Control)

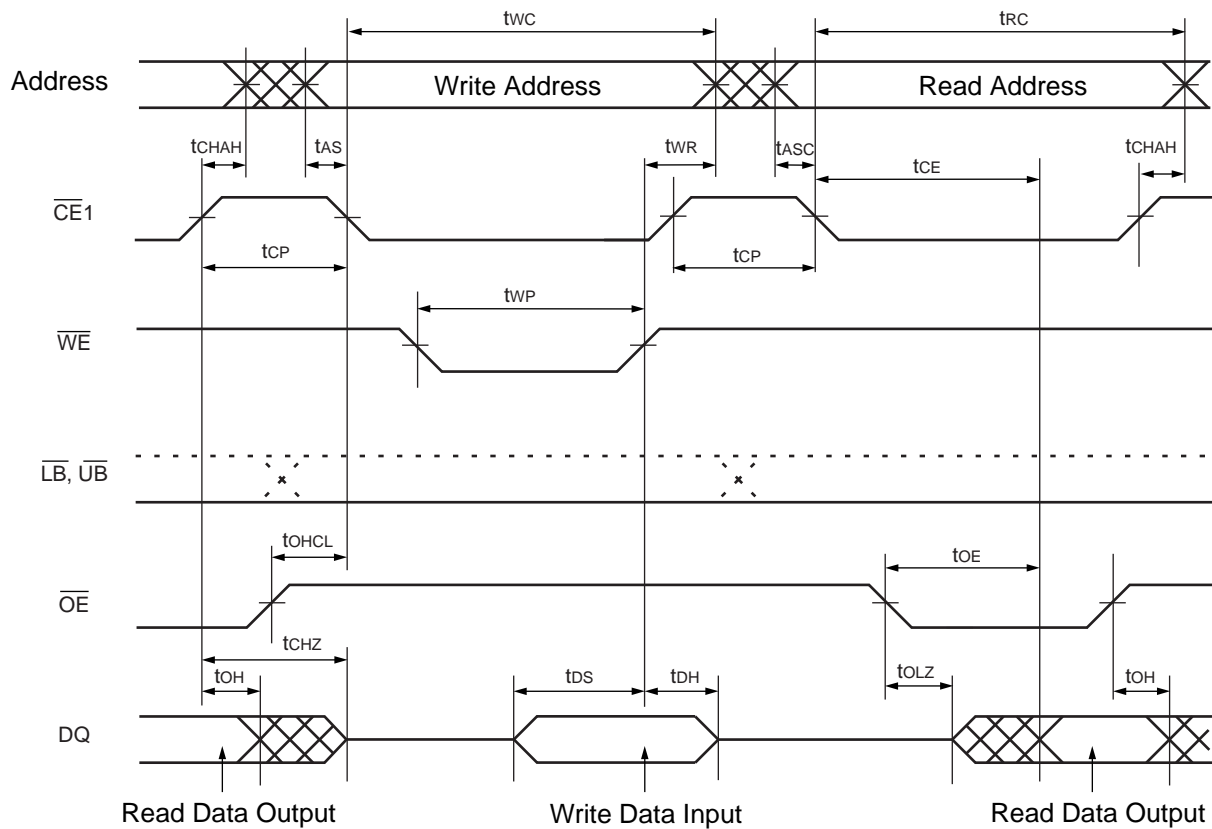


## (12) Asynchronous Read/Write Timing 1-1 ( $\overline{\text{CE1}}$ Control)



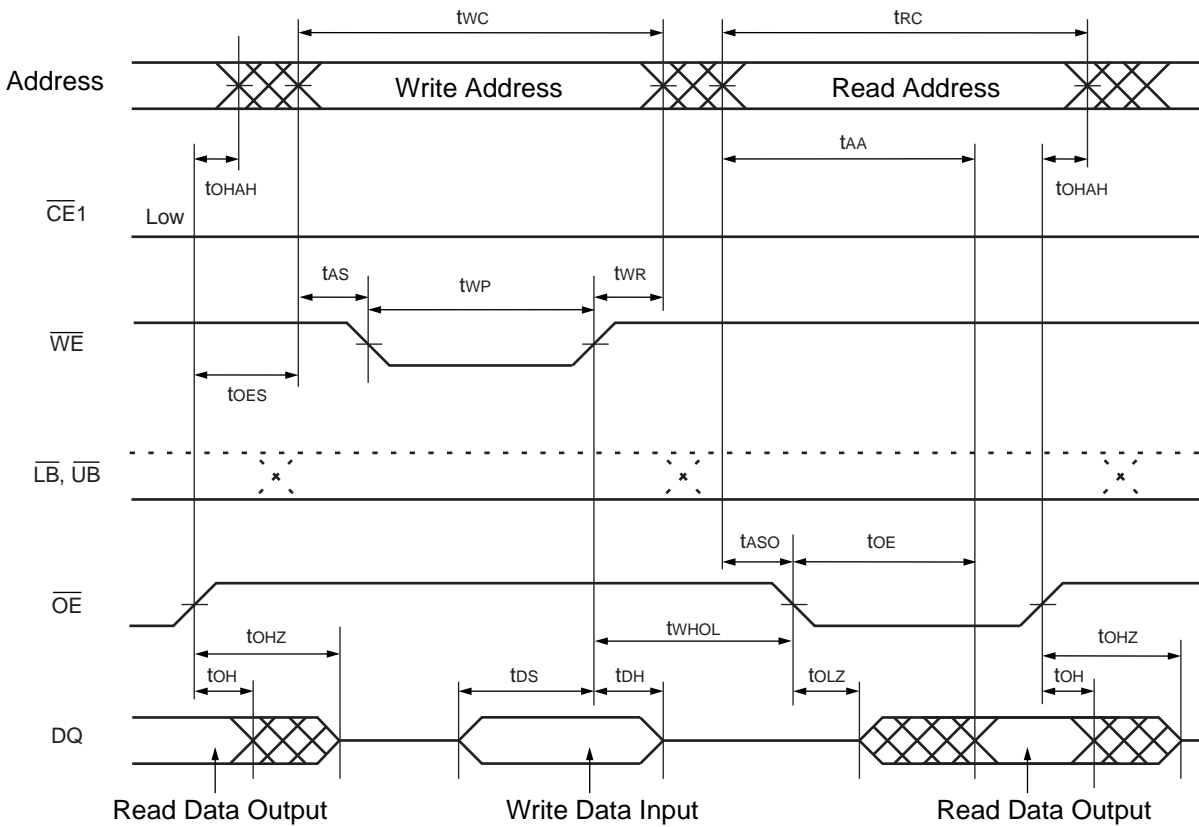
- Notes :
- This timing diagram assumes  $\text{CE2} = \text{H}$  and  $\overline{\text{ADV}} = \text{L}$ .
  - Write address is valid from either  $\overline{\text{CE1}}$  or  $\overline{\text{WE}}$  of last falling edge.

## (13) Asynchronous Read/Write Timing 1-2 ( $\overline{CE1}$ , $\overline{WE}$ , $\overline{OE}$ Control)



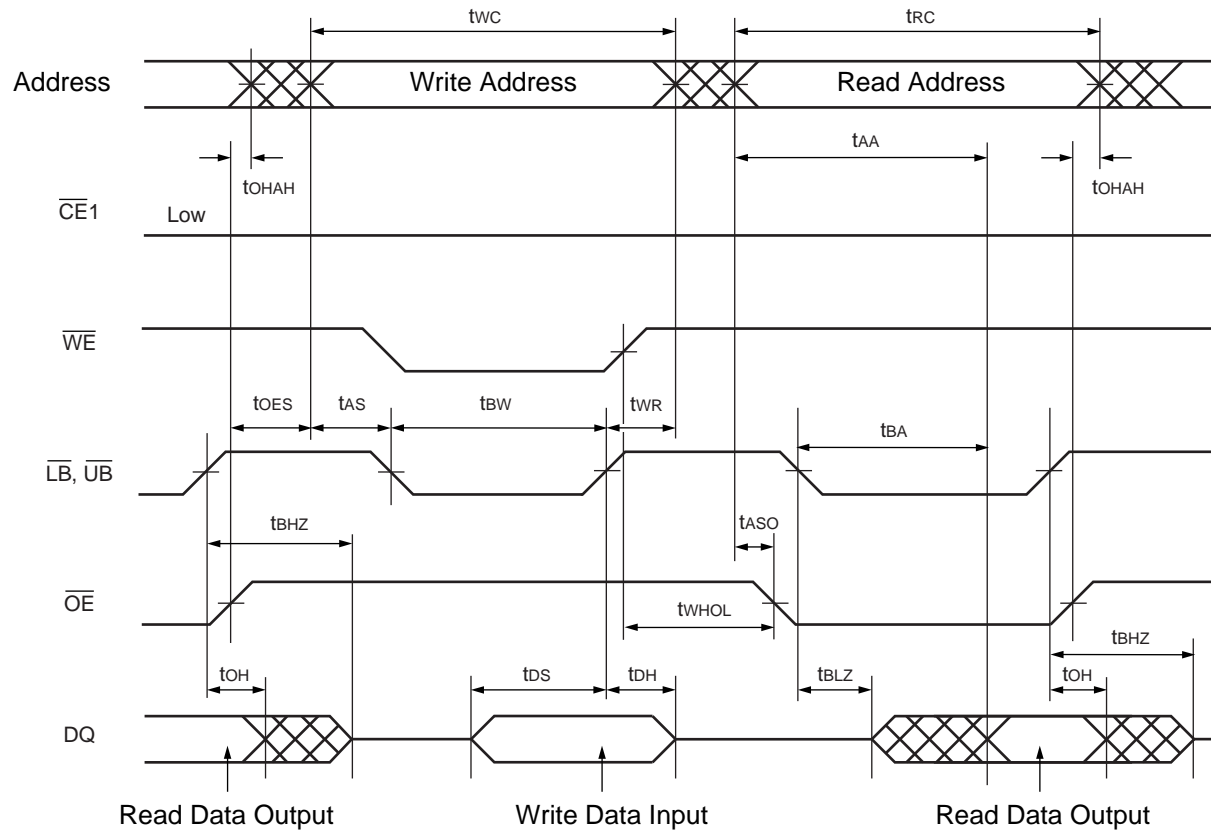
- Notes :
- This timing diagram assumes  $CE2 = H$  and  $\overline{ADV} = L$ .
  - $\overline{OE}$  can be fixed Low during write operation if it is  $\overline{CE1}$  controlled write at Read-Write-Read sequence.

## (14) Asynchronous Read/Write Timing 2 ( $\overline{OE}$ , $\overline{WE}$ Control)



- Notes :
- This timing diagram assumes  $\overline{CE2} = H$  and  $\overline{ADV} = L$ .
  - $\overline{CE1}$  can be tied to Low for  $\overline{WE}$  and  $\overline{OE}$  controlled operation.
  - Read data will be available after  $t_{AA}$  from  $\overline{WE} = H$  if read addresses are not changed from write address.

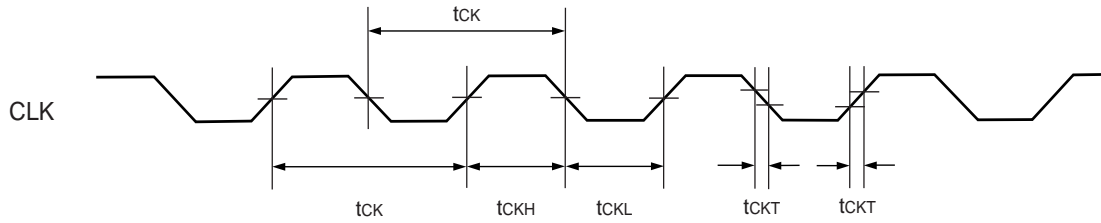
## (15) Asynchronous Read/Write Timing 3 ( $\overline{OE}$ , $\overline{WE}$ , $\overline{LB}$ , $\overline{UB}$ Control)



- Notes :
- This timing diagram assumes  $CE2 = H$  and  $\overline{ADV} = L$ .
  - $\overline{CE1}$  can be tied to Low for  $\overline{WE}$  and  $\overline{OE}$  controlled operation.
  - Read data will be available after  $t_{AA}$  from  $\overline{WE} = H$  if read addresses are not changed from write address.

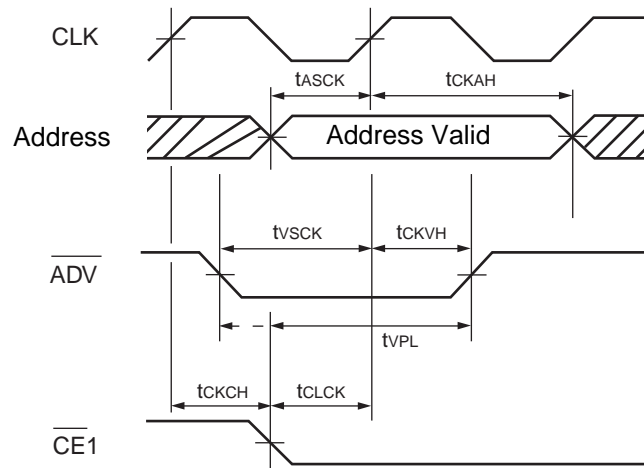


## (16) Clock Input Timing



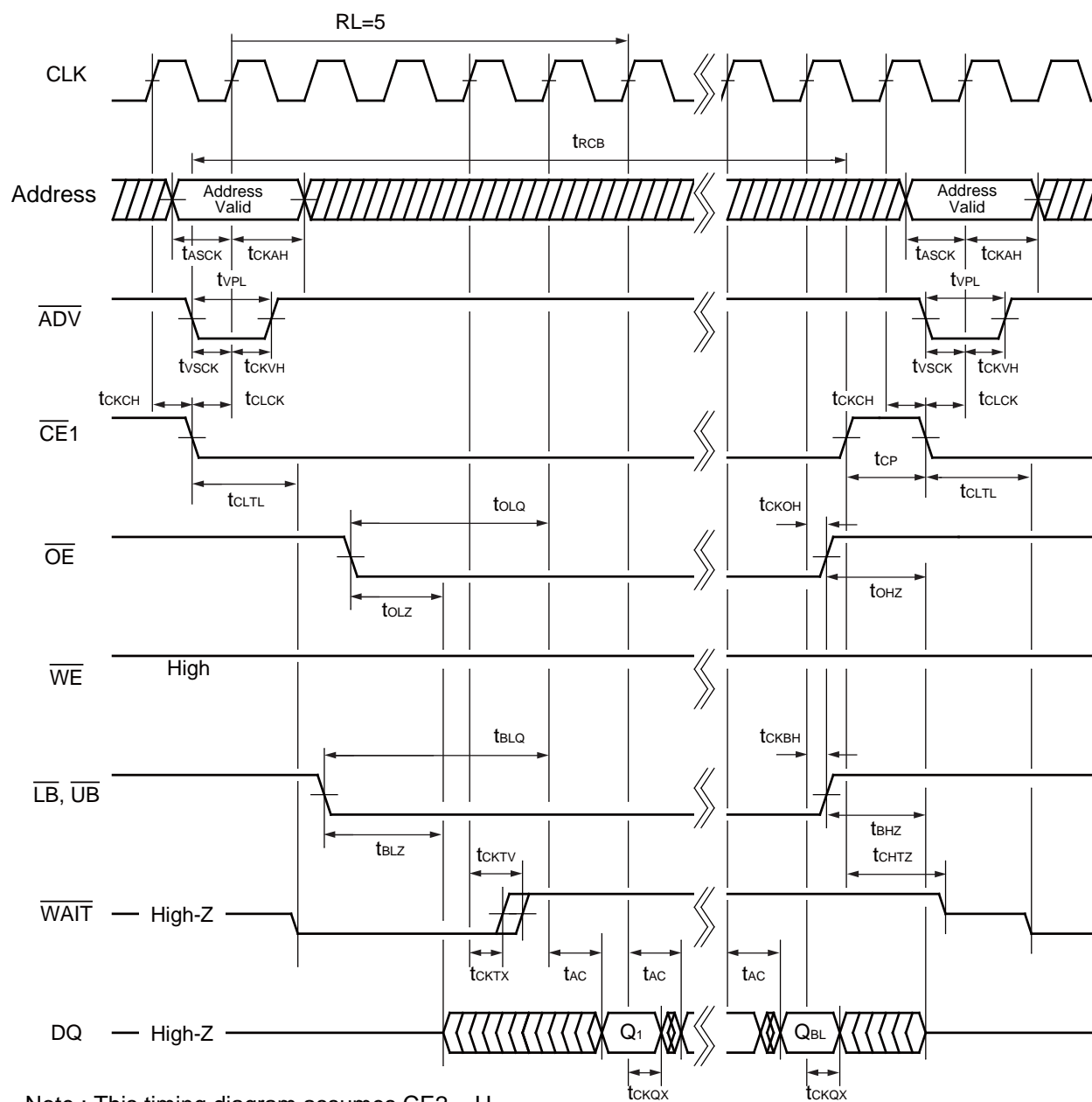
- Notes :
- Stable clock input must be required during  $\overline{CE1} = L$ .
  - $t_{CK}$  is defined between rising clock edges.
  - $t_{CKT}$  is defined between  $V_{IH}$  (Min) and  $V_{IL}$  (Max).

## (17) Address Latch Timing (Synchronous Mode)



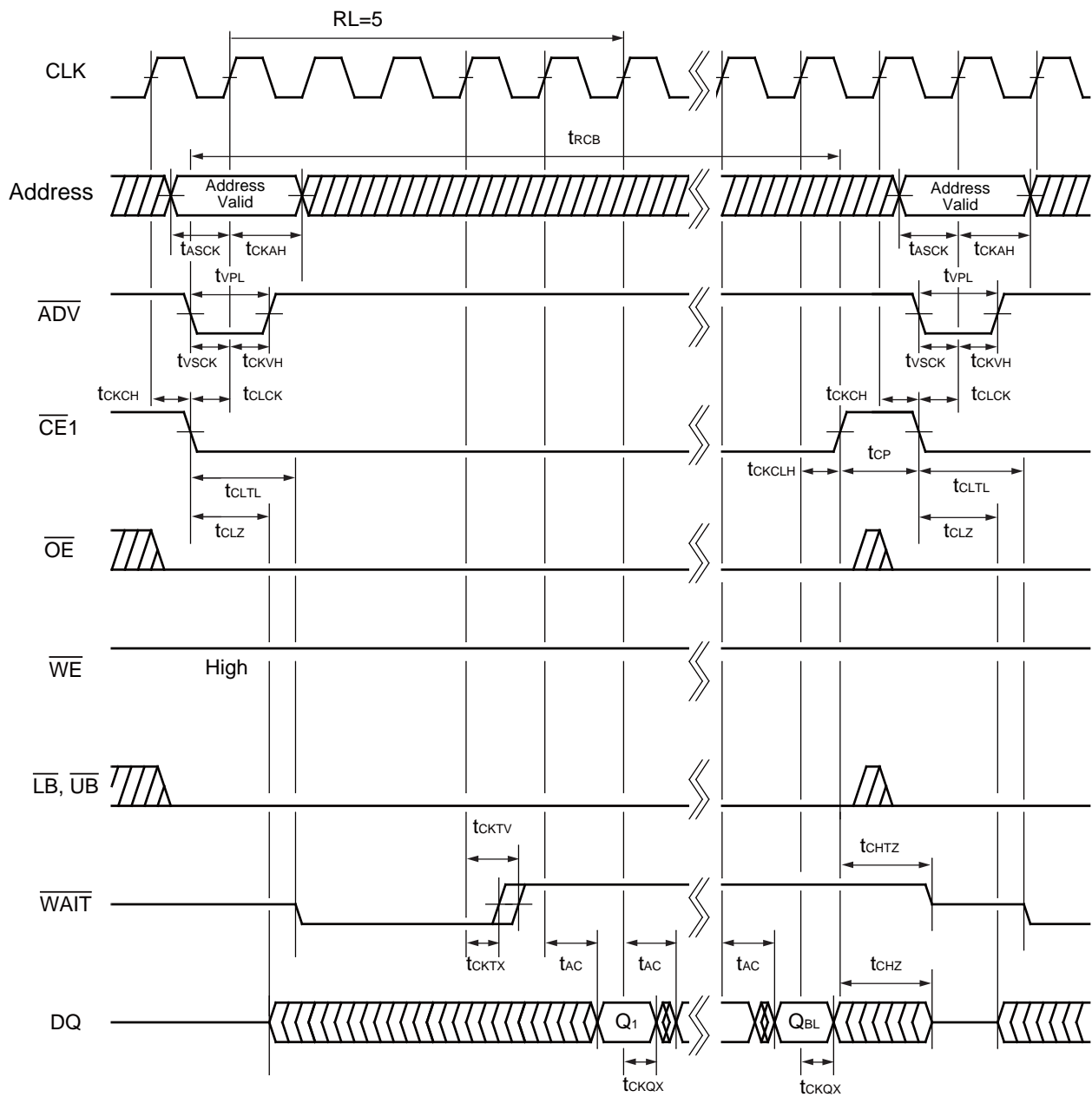
- Notes :
- $t_{VPL}$  is specified from the falling edge of either  $\overline{CE1}$  or  $\overline{ADV}$  whichever comes late.
  - At least one rising clock edge must be input during  $\overline{ADV} = L$ .
  - $t_{ASCK}$ ,  $t_{VSCK}$  and  $t_{CLCK}$  are applied to the 1st valid clock edge during  $\overline{ADV} = L$ .
  - $t_{CKCH}$  is applied to the rising clock edge before address latching.

### (18) Synchronous Read Timing 1 ( $\overline{\text{OE}}$ Control)



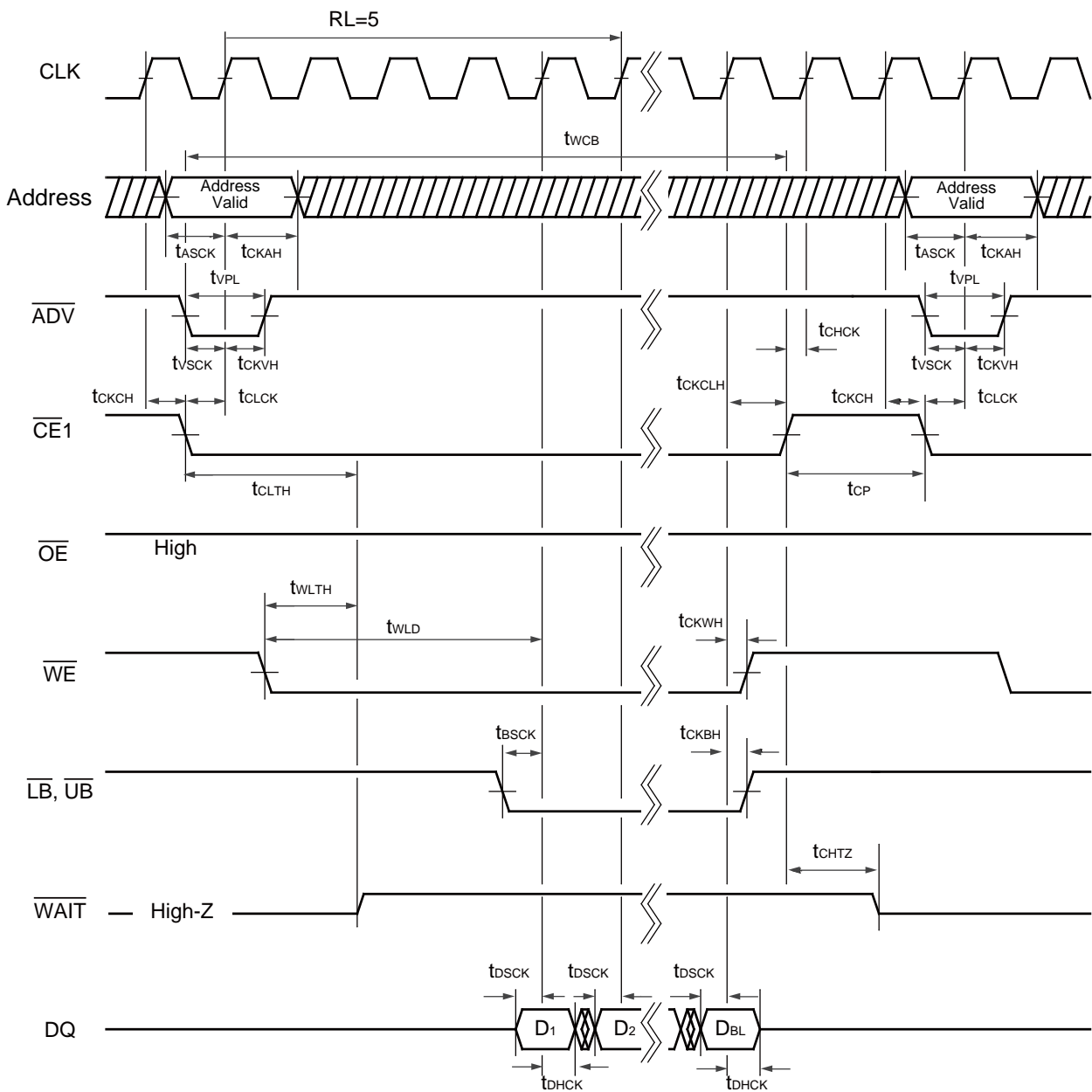
Note : This timing diagram assumes  $CE2 = H$ .

## (19) Synchronous Read Timing 2 ( $\overline{CE1}$ Control)



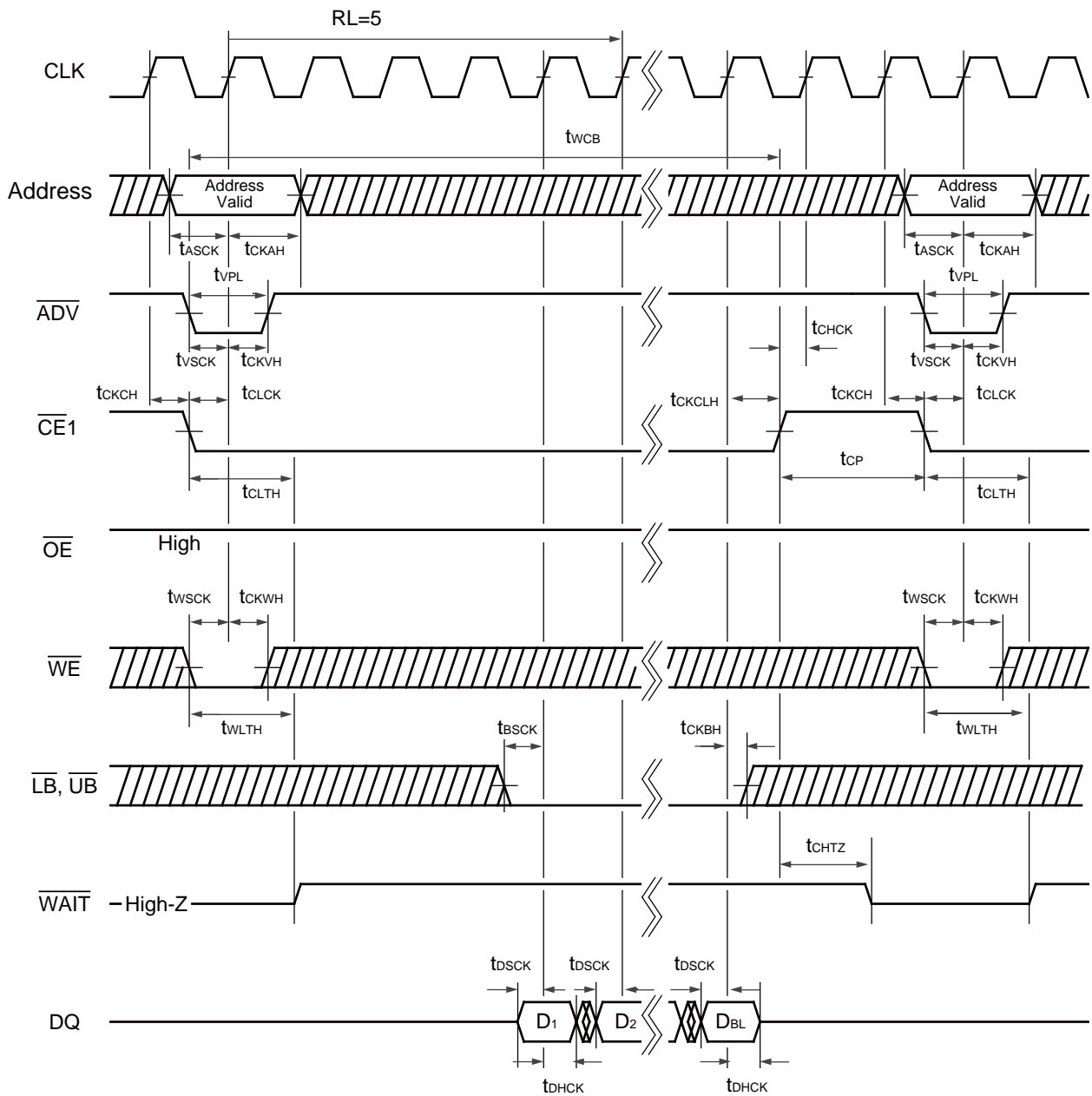
Note : This timing diagram assumes  $CE2 = H$ .

## (20) Synchronous Write Timing 1 ( $\overline{WE}$ Level Control)



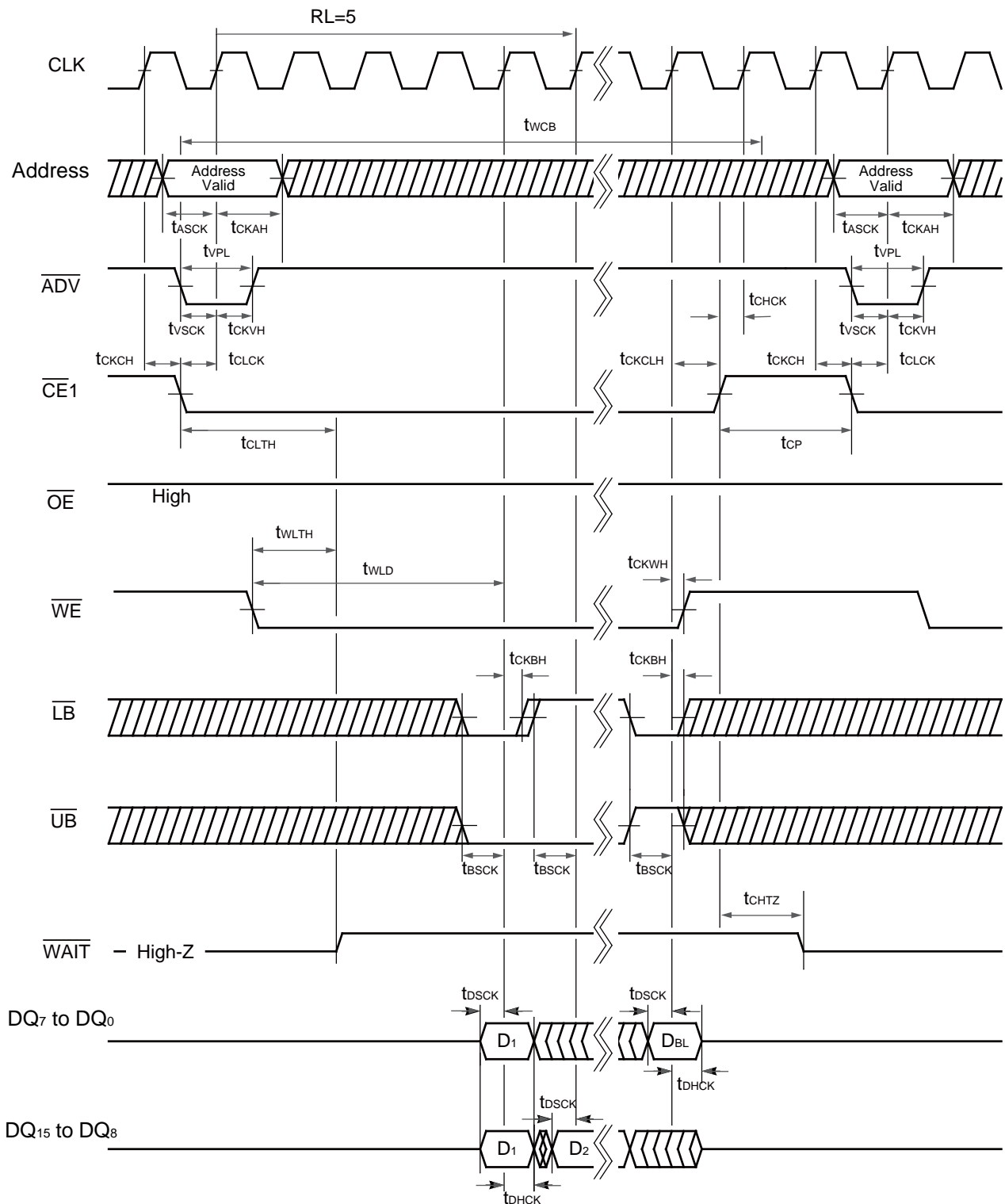
Note : This timing diagram assumes CE2 = H.

## (21) Synchronous Write Timing 2 ( $\overline{WE}$ Single Clock Pulse Control)



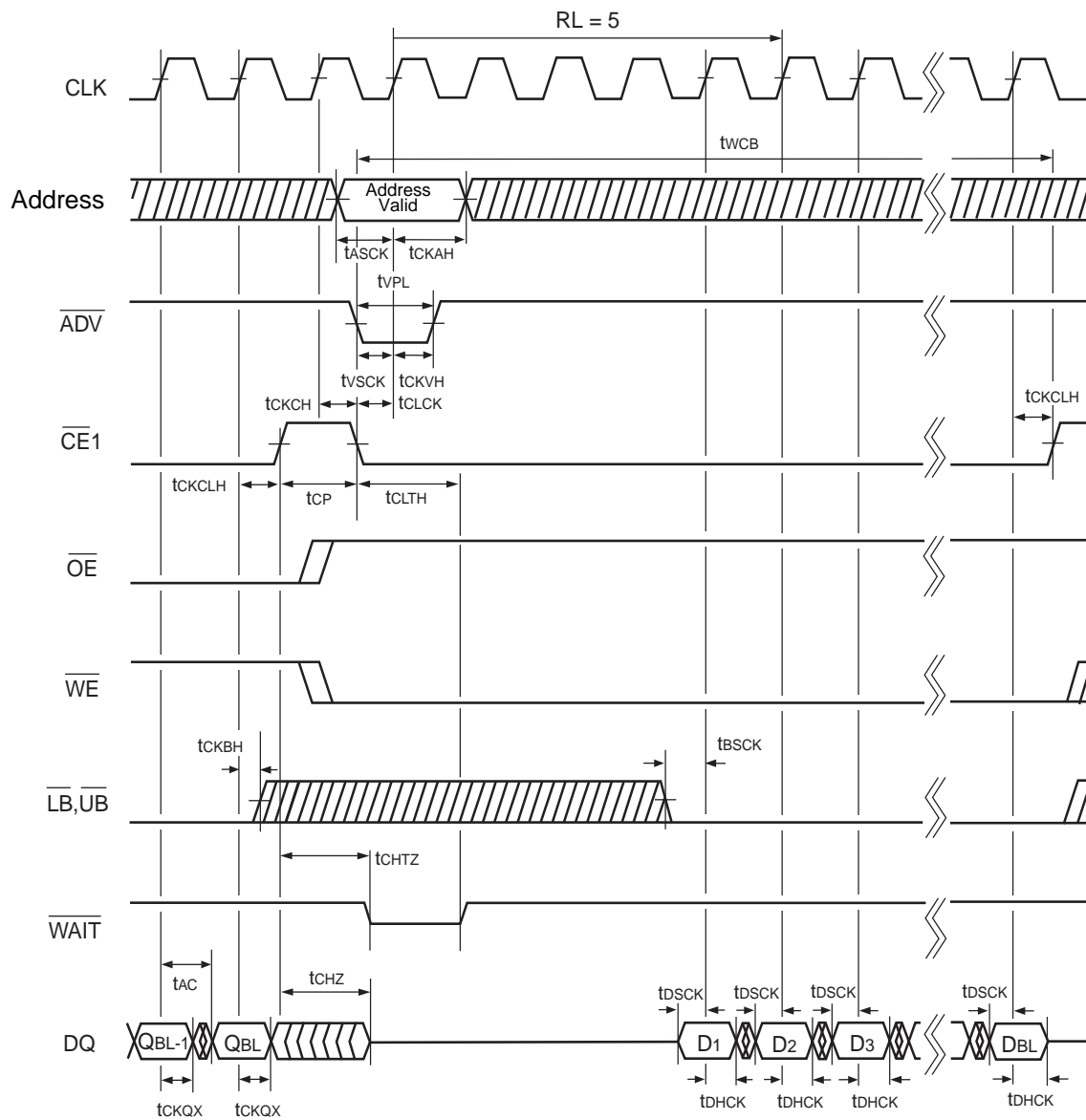
Note : This timing diagram assumes  $CE2 = H$ .

## (22) Synchronous Write Timing 3 ( $\overline{\text{LB}}$ , $\overline{\text{UB}}$ Byte Mask Control)



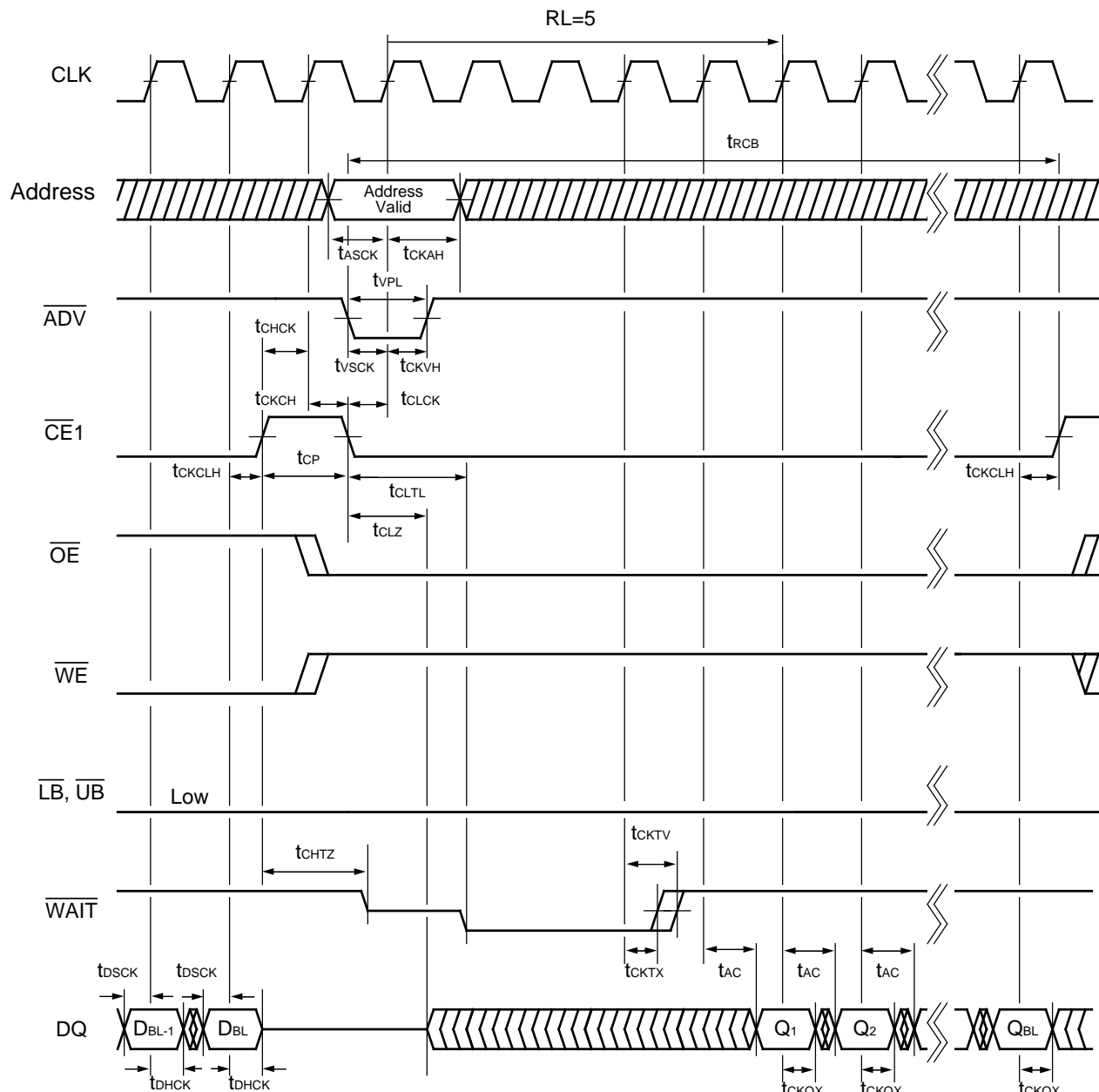
Note : This timing diagram assumes CE2 = H and  $\overline{\text{WE}}$  Level Control.

## (23) Synchronous Read to Write Timing 1 ( $\overline{\text{CE1}}$ Control)



Note : This timing diagram assumes  $\text{CE2} = \text{H}$ .

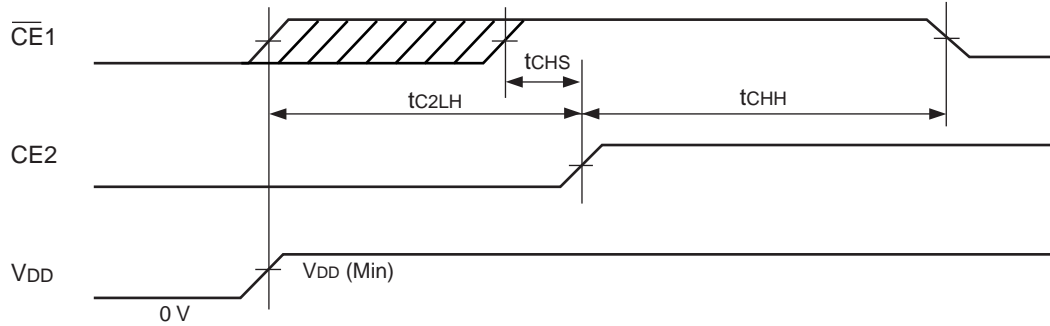
## (24) Synchronous Write to Read Timing 1 ( $\overline{\text{CE1}}$ Control)



Note : This timing diagram assumes  $\text{CE2} = \text{H}$ .

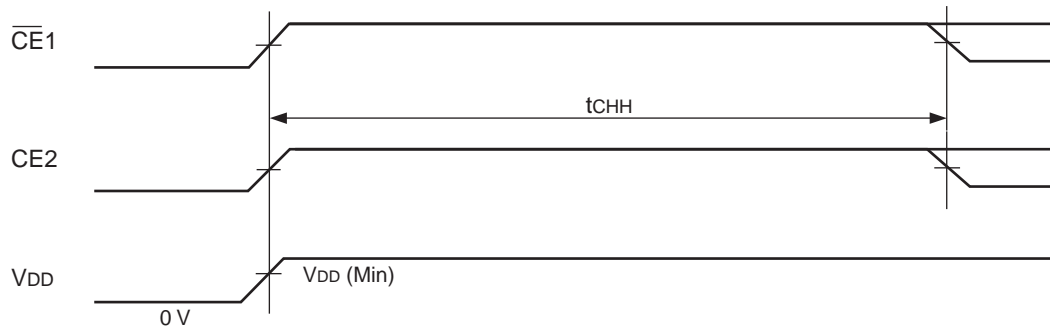


## (25) Power-up Timing 1



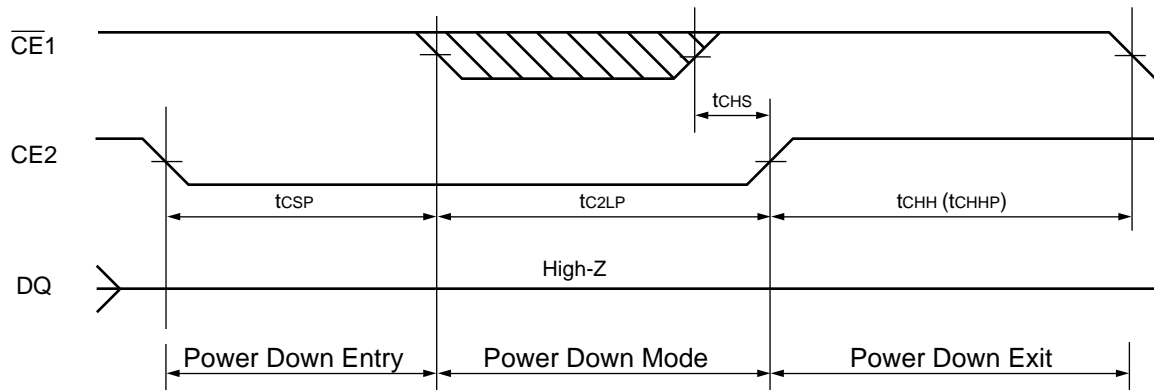
Note : The  $t_{C2LH}$  specifies after  $V_{DD}$  reaches specified minimum level.

## (26) Power-up Timing 2



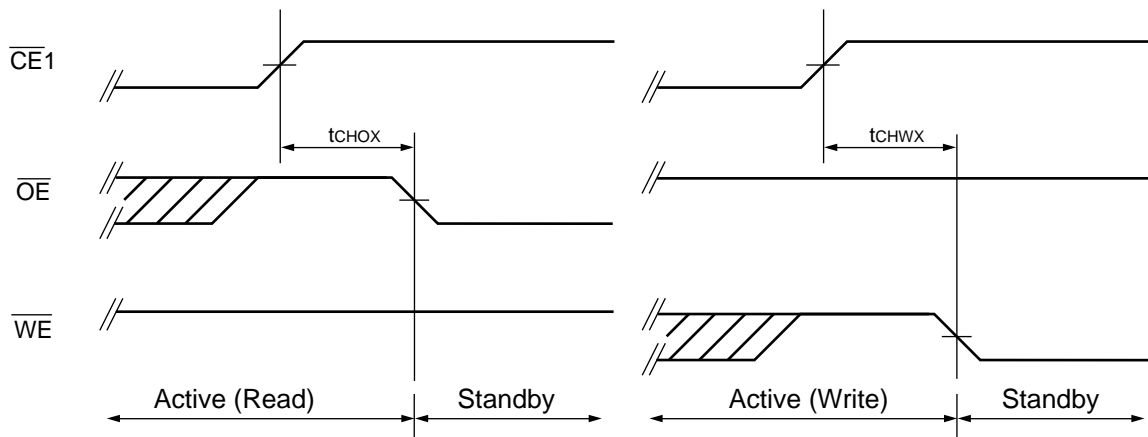
Note : The  $t_{CHH}$  specifies after  $V_{DD}$  reaches specified minimum level and applicable to both  $\overline{CE1}$  and  $CE2$ . If transition time of  $V_{DD}$  (from 0 V to  $V_{DD} (Min)$ ) is longer than 50 ms, (25) Power-up Timing 1 must be applied.

## (27) Power Down Entry and Exit Timing



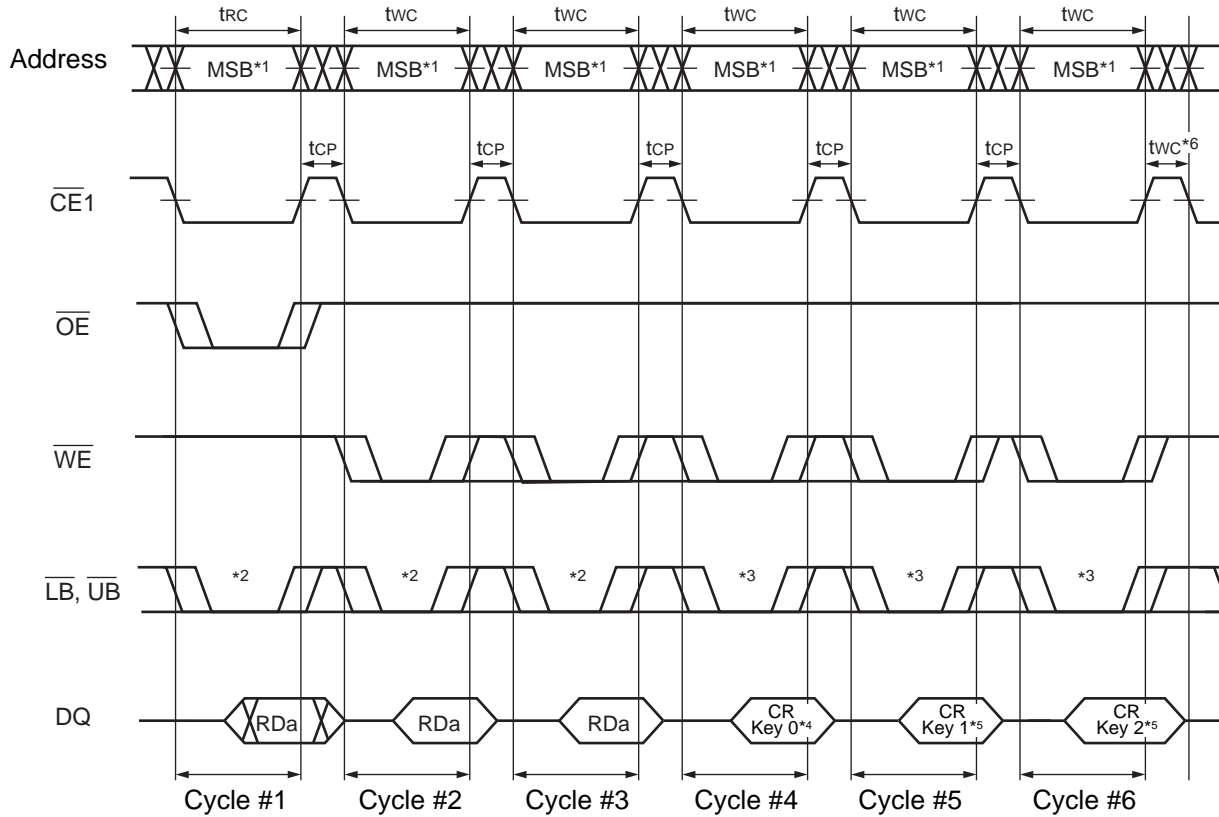
- Notes :
- Power Down mode can be also used as a reset timing if "Power-up Timing" above could not be satisfied and Power Down program was not performed prior to this reset.
  - $\overline{CE2}$  can be brought to Low after the completion of previous Read/Write operation.
  - $\overline{CE2}$  must be kept at High during the specified minimum time of  $t_{CP}$ .

## (28) Standby Entry Timing after Read or Write



Note : Both  $t_{CHOX}$  and  $t_{CHWX}$  define the earliest entry timing for Standby mode.

## (29) Configuration Register Set Timing 1 (Asynchronous Operation)



\*1 : The all address inputs must be High from Cycle #1 to #6.

\*2 : At least either  $\overline{LB}$  or  $\overline{UB}$  must be brought to Low during Cycle #1 to #3.

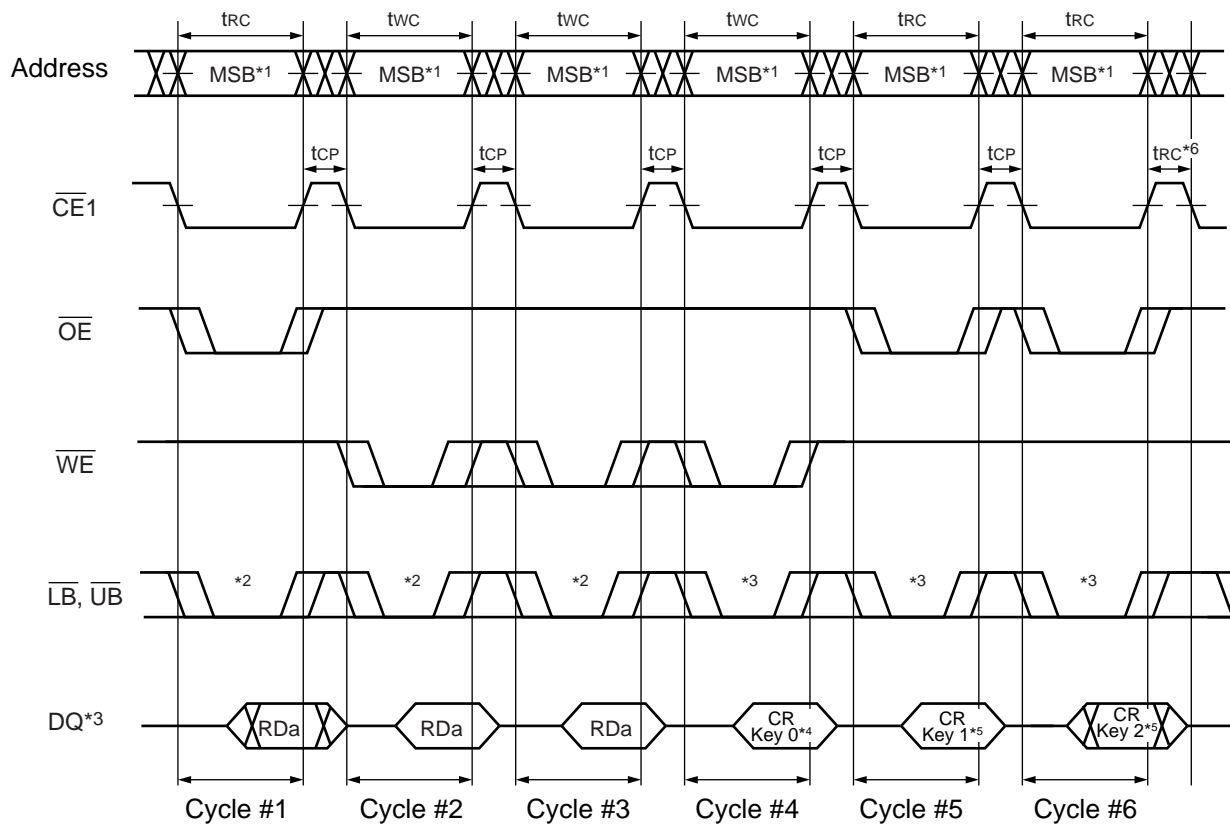
\*3 :  $\overline{LB}$  must be brought to Low in order to input the CR Keys during Cycle #4 to #6.

\*4 : The CR Key 0 must be set "1" for the CR Set as specified in "FUNCTIONAL DESCRIPTION".

\*5 : The CR Keys must conform to the format specified in "FUNCTIONAL DESCRIPTION". If not, any operations and data are not guaranteed.

\*6 : After  $t_{WC}$  following Cycle #6, the Configuration Register Set is completed and returned to the normal operation.

## (30) Configuration Register Verify Timing 1 (Asynchronous Operation)



\*1 : The all address inputs must be High from Cycle #1 to #6.

\*2 : At least either  $\overline{LB}$  or  $\overline{UB}$  must be brought to Low during Cycle #1 to #3.

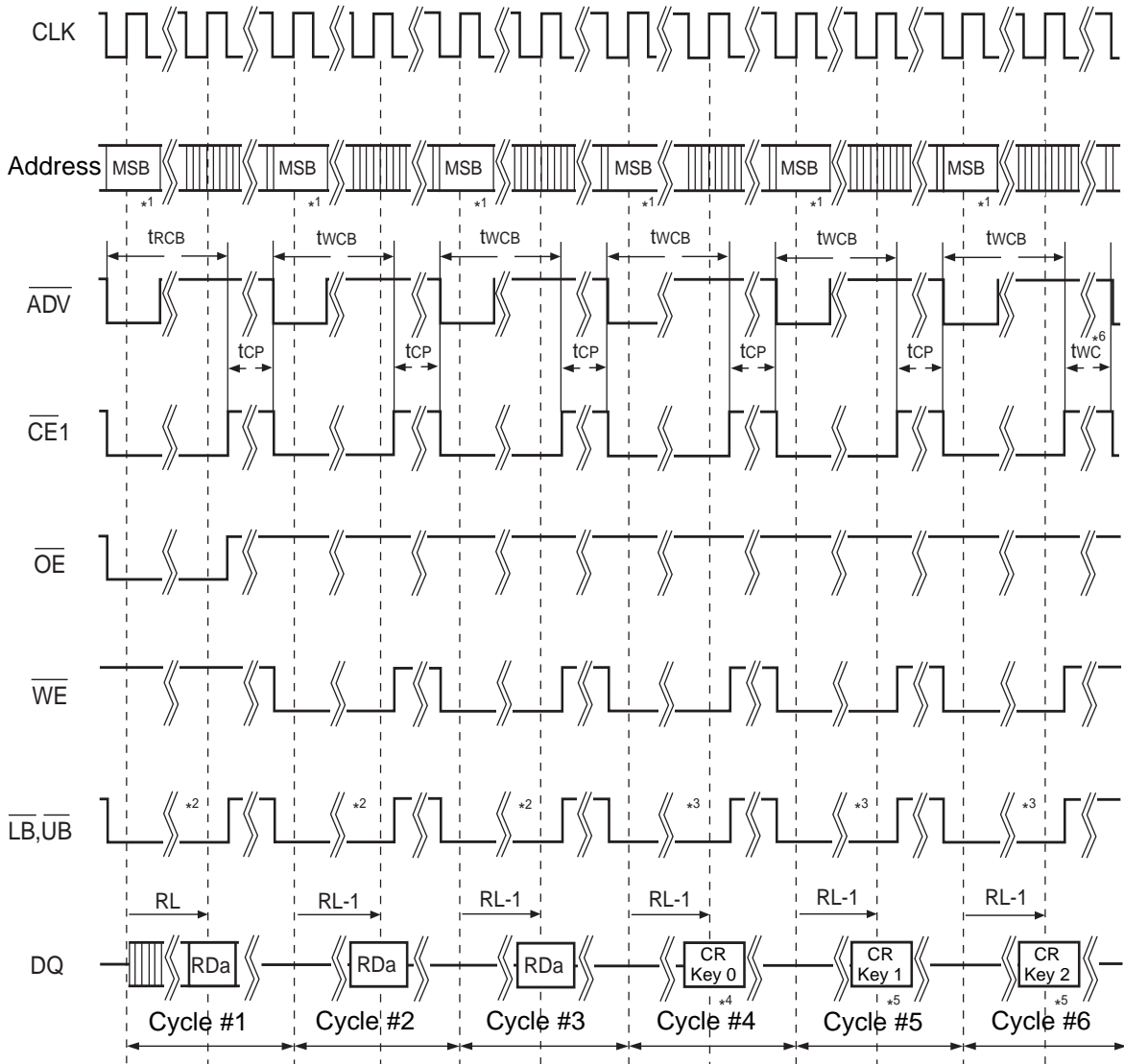
\*3 :  $\overline{LB}$  must be brought to Low in order to input or output the CR Keys during Cycle #4 to #6.

\*4 : The CR Key 0 must be set "0" for the CR Verify as specified in "■FUNCTIONAL DESCRIPTION".

\*5 : The CR Keys must conform to the format specified in "■FUNCTIONAL DESCRIPTION". If not, any operations and data are not guaranteed.

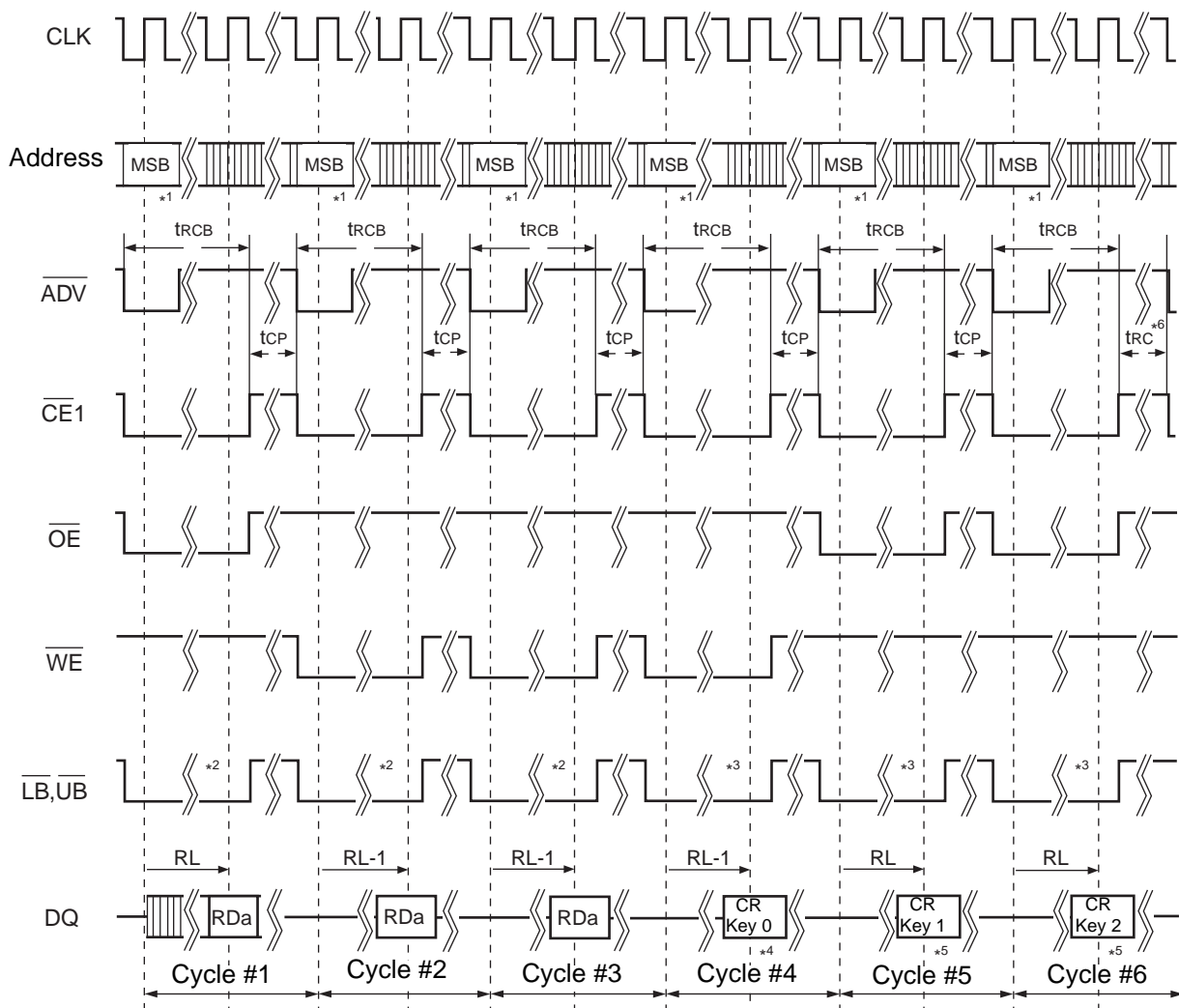
\*6 : After  $t_{RC}$  following Cycle #6, the Configuration Register Verify is completed and returned to the normal operation.

## (31) Configuration Register Set Timing 2 (Synchronous Operation)



- \*1 : The all address inputs must be High from Cycle #1 to #6.
- \*2 : At least either  $\overline{LB}$  or  $\overline{UB}$  must be brought to Low during Cycle #1 to #3.
- \*3 :  $\overline{LB}$  must be brought to Low in order to input the CR Keys during Cycle #4 to #6.
- \*4 : The CR Key 0 must be set "1" for the CR Set as specified in "■ FUNCTIONAL DESCRIPTION".
- \*5 : The CR Keys must conform to the format specified in "■ FUNCTIONAL DESCRIPTION". If not, any operations and data are not guaranteed.
- \*6 : After  $t_{wC}$  following Cycle #6, the Configuration Register Set is completed and returned to the normal operation.

## (32) Configuration Register Verify Timing 2 (Synchronous Operation)

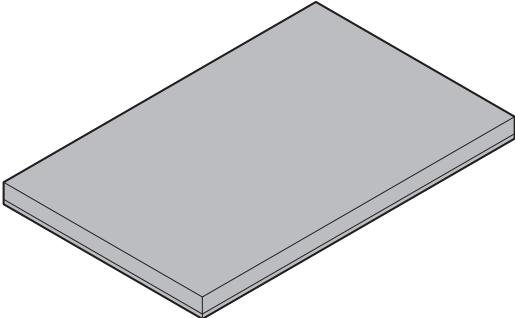


- \*1 : The all address inputs must be High from Cycle #1 to #6.
- \*2 : At least either  $\overline{LB}$  or  $\overline{UB}$  must be brought to Low during Cycle #1 to #3.
- \*3 :  $\overline{LB}$  must be brought to Low in order to input or output the CR Keys during Cycle #4 to #6.
- \*4 : The CR Key 0 must be set "0" for the CR Verify as specified in "■FUNCTIONAL DESCRIPTION".
- \*5 : The CR Keys must conform to the format specified in "■FUNCTIONAL DESCRIPTION". If not, any operations and data are not guaranteed.
- \*6 : After  $t_{RC}$  following Cycle #6, the Configuration Register Verify is completed and returned to the normal operation.

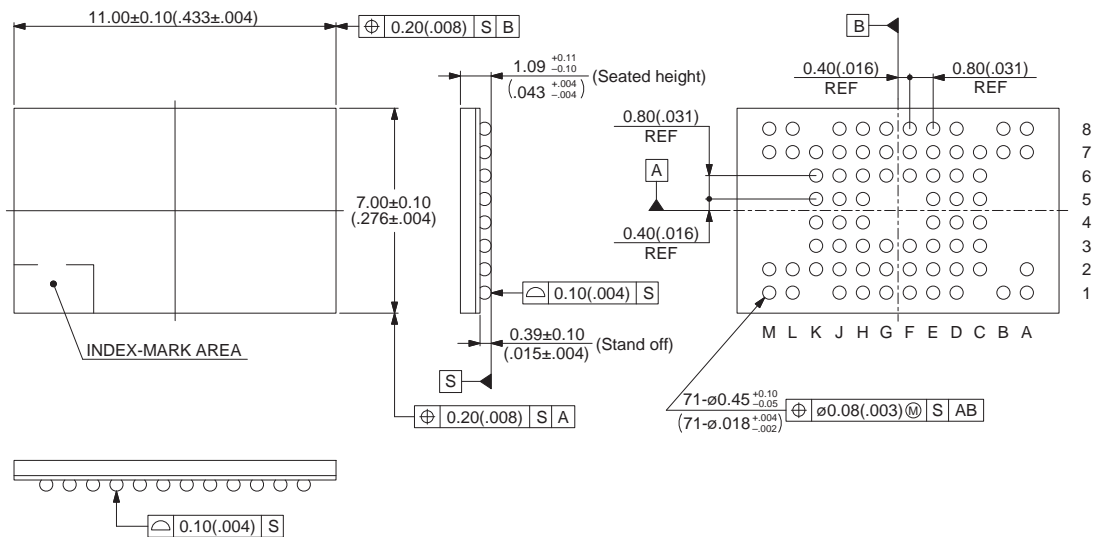
## ■ ORDERING INFORMATION

Part Number	Package
MB82DBS08164D-70LTBG	71-ball plastic FBGA (BGA-71P-M03)

## ■ PACKAGE DIMENSIONS

<p>71-ball plastic FBGA</p>  <p>(BGA-71P-M03)</p>	Ball pitch	0.80 mm
	Package width × package length	7.00 × 11.00 mm
	Lead shape	Soldering ball
	Sealing method	Plastic mold
	Ball size	Ø0.45 mm
	Mounting height	1.20 mm Max.
	Weight	0.14 g

71-ball plastic FBGA  
(BGA-71P-M03)



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Dimensions in mm (inches).  
Note: The values in parentheses are reference values.

Please check the latest Package dimension at the following URL.  
<http://edevic.fujitsu.com/package/en-search/>



**MEMO**

**MEMO**

**MEMO**

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